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Test Specification for 100 Gbit/s and 400 Gbit/s PAM4 Optical Module at 100 Gbit/s per Lane

Test Specification for 100Gb/s and 400Gb/s PAM4-OM-at100Gb/s-PL-01.0

September 8, 2022

Implementation Agreement Created and Approved by

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Work Group: **Plugfest Work Group**

TITLE: **Test Specifications for 100 Gbit/s and 400 Gbit/s PAM4 Optical Modules at 100 Gbit/s per Lane**

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Source Photonics
YOFC
ZTE

ABSTRACT: This test specification applies to 100 Gbit/s and 400 Gbit/s PAM4 optical modules at 100 Gbit/s per lane. In this document, test items include the optical interfaces, electrical interfaces, power consumption, management interfaces, and interconnection and interworking.

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3 Document Revision History

Table 3-1 Document revision history

Document	Date	Revisions/Comments
Test Specification for 100Gb/s and 400Gb/s PAM4-OM-at100Gb/s-PL-01.0	September 8, 2022	Initial release

4 Abbreviation

AOP：Average Optical Power

BER：Bit Error Rate

BERT：Bit Error Rate Tester

CRU：Clock Recovery Unit

CTLE：Continuous Time Linear Equalizer

DUT：Device Under Test

EF：Encircled Flux

EH：Eye Height

EW：Eye Width

EOJ：Even-Odd Jitter

FEC：Forward Error Correction

HCB：Host Compliance Board

I2C：Inter-Integrated Circuit

I2CMCI：I2C-Based Management Communication Interface

MCB：Module Compliance Board

NRZ：Non-return-to-zero

O/E：Optical to Electrical Converter

OMA：Optical Modulation Amplitude

OSA：Optical Spectrum Analyzer

OSC：Oscilloscope

PAM4：4 Pulse Amplitude Modulation

PRBS：Pseudo Random Binary Sequence

RIN_xOMA：Relative Intensity Noise Optical Modulation Amplitude

RMS：Root Mean Square

SMSR：Side Mode Suppression Ratio

TDECQ: Transmitter and Dispersion Eye Closure Quaternary

UBHPJ：Uncorrelated Bounded High Probability Jitter

UUGL： Uncorrelated Unbounded Gaussian Jitter

5 General

5.1 Scope

5.2 Test Environment Requirements

The test environment requirements are as follows:

- Temperature：15℃~35℃
- Relative humidity：45%~75%
- Atmospheric pressure：86kPa~106kPa

5.3 Test Instrument Requirements

The test instruments should be within the effective calibration period. Except for special declaration, the accuracy of test instruments should be one order of magnitude higher than the accuracy of the measured parameters.

5.4 Other Requirements

1. Except for special declaration:

- The modulation format of the BERT output signal is PAM4.
- DUT in the test block diagram refers to the optical module under test.
- The total output service rate for BERT is 106.25Gb/s for 100Gb/s optical modules and 425Gb/s for 400Gb/s optical modules.
- In all tests, power on the DUT and ensure that it works properly.
- In all tests, ensure that the test instrument is in normal working condition. For example, ensure that the power input to the test instrument is within its working range.

2. There are two ways to test each lane individually. One is by turning on only one laser and the other is by connecting to an external wavelength multi/demultiplexer.

a. Turning on only one laser is usually achieved via software protocol.

b. Connecting to an external wavelength multi/demultiplexer is shown in Figure 5-1. And the adjacent isolation of the multi/demultiplexer is not less than 30.00dB. If the test involves optical power measurement, the power calibration is a must.

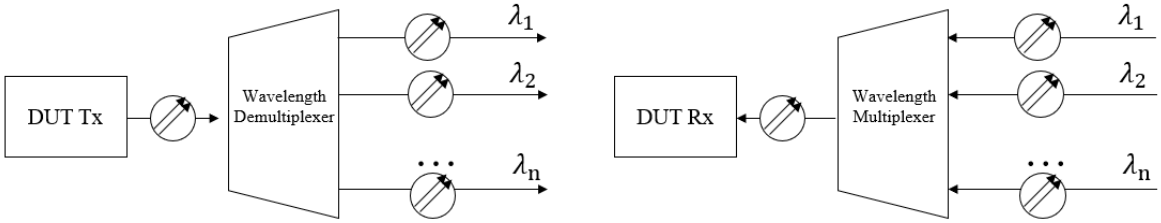


Figure 5-1 The diagram of connecting to an external wavelength multi/demultiplexer

6 Optical Interfaces

The clause is organized into several methods for the industry to reference in optical interface testing.

6.1 Test Patterns for Optical Parameters

Table 6-1 Test patterns

Pattern	Pattern Description		Defined in[a]
Square wave	Square wave (8 threes, 8 zeroes)		120.5.11.2.4
3	PRBS31Q		120.5.11.2.2
4	PRBS13Q		120.5.11.2.1
5	100G	Scrambled idle encoded by RS-FEC	82.2.11.91
	400G	Scrambled idle	119.2.4.9
6	SSPRQ		120.5.11.2.3
[a]These sub-clauses make reference to relevant clauses of IEEE Std 802.3-2018.			

Table 6-2 Test pattern definitions and related subclauses

Parameter	Pattern		Location	Reference
Signaling rate	6		**6.2**	IEEE 802.3bs 120E.3.1.1
Frequency offset tolerance	Valid 100GBASE-Rsignal		**6.3**	IEEE 802.3cu 140.6.2 IEEE 802.3bs 124.7.2 IEEE 802.3cu 151.7.2
	Valid 400GBASE-Rsignal			
Center wavelength	100G	Square wave, 3, 4, 5, 6, or valid 100GBASE-Rsignal	**6.4**	IEC 61280-1-3 8.2
	400G	Square wave, 3, 4, 5, 6, or valid 400GBASE-Rsignal		

Parameter	Pattern		Location	Reference
SMSR	100G	3, 5, 6, or valid 100GBASE-Rsignal	**6.5**	IEC 61280-1-3 8.8
	400G	3, 5, 6, or valid 400GBASE-Rsignal		
RMS spectral width	100G	3, 5, 6, or valid 100GBASE-Rsignal	**6.6**	IEC 61280-1-3 8.5
	400G	3, 5, 6, or valid 400GBASE-Rsignal		
Average optical power	100G	3, 5, 6, or valid 100GBASE-Rsignal	**6.7**	IEC 61280-1-1
	400G	3, 5, 6, or valid 400GBASE-Rsignal		
Outer optical modulation amplitude (OMA_{outer})	4 or 6		**6.8**	IEEE 802.3-2018 121.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6		**6.10**	IEEE 802.3-2018 121.8.5
Average launch power of OFF transmitter	3, 5, 6, or valid 100GBASE-Rsignal		**6.12**	IEC 61280-1-1
	3, 5, 6, or valid 400GBASE-Rsignal			
Extinction ratio	4 or 6		**6.14**	IEEE 802.3bs 121.8.6
Transmitter transition time	Square wave or 6		**6.15**	IEEE 802.3cu-2021 151.8.10
RINxOMA	Square wave		**6.16**	IEEE 802.3-2018 52.9.6
Optical return loss tolerance	3, 5, 6, or valid 100GBASE-Rsignal		**6.18**	YD/T 2798.2-2020 5.10
Transfer delay	Square wave, 3, 4, 5, 6, or valid 100GBASE-Rsignal		**6.19**	IEEE 802.3bs 116.4
	Square wave, 3, 4, 5, 6, or valid 400GBASE-Rsignal			
Transmitter eye closure for PAM4 (TECQ)	6		**6.21**	IEEE 802.3cu-2021 151.8.6
Over/under-shoot	6		**6.23**	IEEE 802.3cu, 140.7.5b
Transmitter power excursion	6		**6.24**	IEEE 802.3cu, 140.7.5c, 151.8.8

Parameter	Pattern	Location	Reference
Damage threshold	3 or 5	**6.25**	IEEE 802.3cu 140.6.2 IEEE 802.3bs 124.7.2 IEEE 802.3cu 151.7.2
Average receive power	3 or 5	**6.26**	
Receive power (OMA_{outer})	3 or 5	**6.27**	NA
Stressed receiver sensitivity	3 or 5	**6.30**	IEEE 802.3bs 121.8.9
Receiver sensitivity (OMA_{outer})	3 or 5	**6.29**	IEEE 802.3cu 140.7.9 IEEE 802.3cu 151.8.12
Maximum skew	Valid 100GBASE-Rsignal	**6.33**	IEEE 802.3bs 116.5
	Valid 100GBASE-Rsignal		
Maximum skew variation	Valid 100GBASE-Rsignal	**6.34**	IEEE 802.3bs 116.5
	Valid 100GBASE-Rsignal		
Receiver sensitivity	3 or 5	**6.35**	IEEE 802.3-2018 121.8.8
Receiver sensitivity with fiber propagation	3 or 5	**6.36**	IEEE 802.3cu 140.7.9 IEEE 802.3cu 151.8.12
Interzone BER	3 or 5	**6.37**	NA
Rx_LOS assert optical power & Rx_LOS de-assert optical power & LOS hysteresis	Square wave, 3, 4, 5, 6, or valid 100GBASE-Rsignal	**6.38**	NA
	Square wave, 3, 4, 5, 6, or valid 400GBASE-Rsignal		
Transmitter reflectance	NA	**6.17**	YD/T 2798.2-2020 6.4
Encircled flux	NA	**6.13**	IEC 61280-1-4
Difference in launch power between any two lanes (OMA_{outer})	3, 5, 6, or valid 100GBASE-Rsignal 3, 5, 6, or valid 400GBASE-Rsignal	**6.20**	IEC 61280-1-1 IEEE 802.3bs 121.8.4
|TDECQ – TECQ|(Max)	6	**6.22**	NA
Receiver reflectance	NA	**6.28**	YD/T 2798.2-2020 6.4

Parameter	Pattern	Location	Reference
Receive overload power (AOP)	3, 5, 6, or valid 100GBASE-Rsignal 3, 5, 6, or valid 400GBASE-Rsignal	**6.31**	NA
Receive overload power (OMA_{outer})	3, 5, 6, or valid 100GBASE-Rsignal 3, 5, 6, or valid 400GBASE-Rsignal	**6.32**	NA

6.2 Signaling Rate

6.2.1 Definition

The **'signaling rate'** indicates the number of symbols transmitted through a lane per unit time; that is, the signal transmission rate after modulation. The **'signaling rate'** can be expressed in either of the following ways: (1) The symbol rate in baud, which indicates the number of symbols transmitted per unit time; (2) The data transmission rate in bit/s or bps, which indicates the amount of information transmitted per second.

6.2.2 Block Diagram

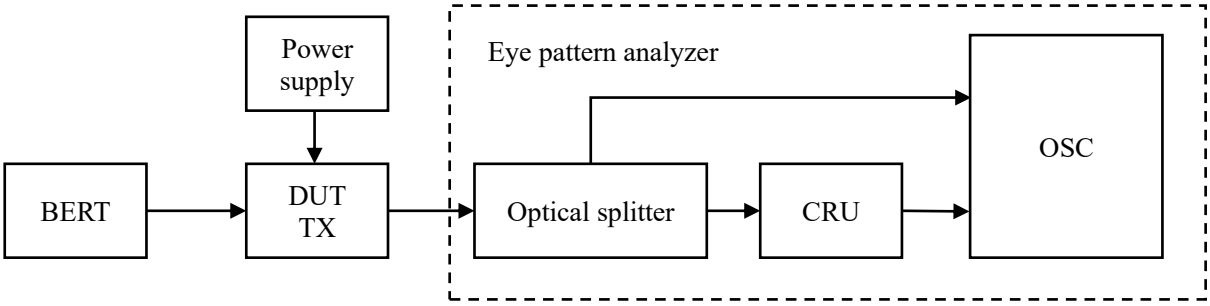


Figure 6-1 Signal rate test

6.2.3 Test Steps

a Connect the test system according to Figure 6-1.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

Note: The amplitude for the **BERT** is advised to be set at 600mV.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by turning on only one laser under test or by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Read the **'signaling rate'** on the **Eye pattern analyzer**.

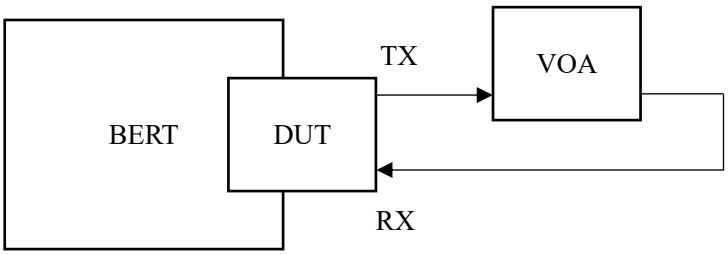
e When for a multi-lane optical module, repeat the test for other lanes.

6.3 Frequency Offset Tolerance

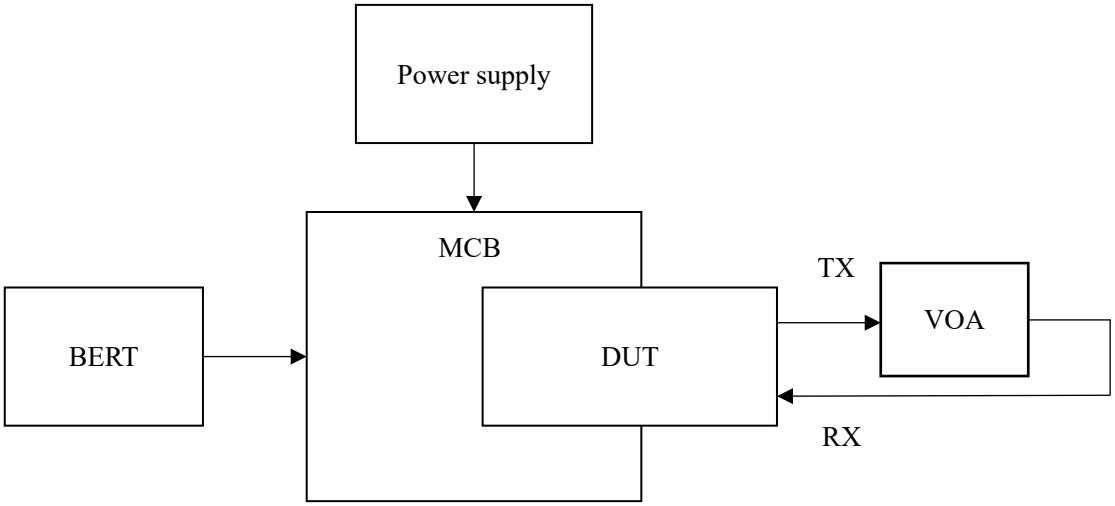
6.3.1 Definition

The **'frequency offset tolerance'** refers to the capability of an electrical or optical port of an optical module to correctly receive signals within a certain frequency offset range.

6.3.2 Block Diagram



a **BERT** can be directly connected to the module



b **BERT** cannot be directly connected to the module

Figure 6-2 Frequency offset tolerance test

6.3.3 Test Steps

a Connect the test system according to Figure 6-2.

b Set the output service rate, modulation format, amplitude, test pattern, output frequency offset and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

Note:

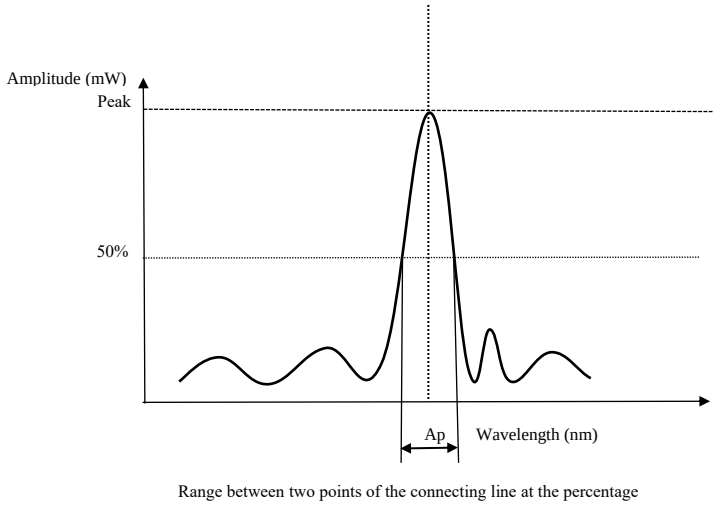
- The amplitude for the **BERT** is advised to be set at 600mV.
- Output frequency offset is advised to select six test points: –100 ppm, –60 ppm, –20 ppm, +20 ppm, +60 ppm, and +100 ppm.
- The frequency offset adjustment rate is advised to be set at 5 ppm/s, 20 ppm/s, 50 ppm/s, and 100 ppm/s.

c Check whether the BER of the **DUT** meets the requirement and read the packet loss rate, and alarm information about the **DUT** on **BERT**.

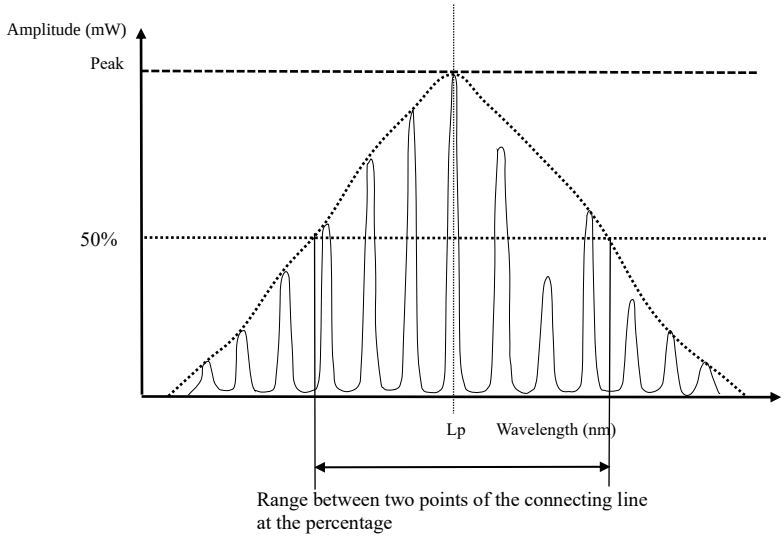
6.4 Center Wavelength

6.4.1 Definition

The **'center wavelength'** is also called "half-power mid-point," which is the average of two optical wavelengths at which the spectral radiant intensity is 50% of the maximum value. The unit is nm. Figure 6-3(a) and Figure 6-3(b) show the center wavelength test principles for single-longitudinal mode laser and multi-longitudinal mode laser, respectively.



a Single-longitudinal mode laser



b Multi-longitudinal mode laser

Figure 6-3 Center wavelength test principles

6.4.2 Block Diagram

Figure 6-4 Center wavelength test

6.4.3 Test Steps

a Connect the test system according to Figure 6-4.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

Note: The amplitude for the **BERT** is advised to be set at 600mV.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by turning on only one laser under test or by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Read the **'center wavelength'** on OSA.

Note: Set the **OSA** to work in vacuum mode before reading the result.

e When for a multi-lane optical module, repeat the test for other lanes.

6.5 SMSR

6.5.1 Definition

For a single-longitudinal mode laser, the **'SMSR'** is defined as the ratio of the main longitudinal mode peak optical power to the secondary maximum longitudinal mode peak optical power. The unit is dB. Figure 6-5 shows the '**SMSR**' test principles for the single-longitudinal mode laser.

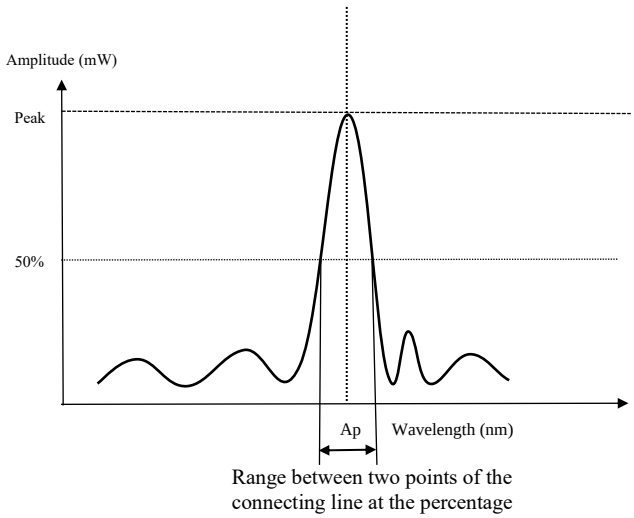


Figure 6-5 SMSR test principles for the single-longitudinal mode laser

6.5.2 Block Diagram

Figure 6-6 SMSR test

6.5.3 Test Steps

a Connect the test system according to Figure 6-6.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c Ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer. And for a multi-lane optical module, all other lanes are in operation using the same test pattern.

d Read the **'SMSR'** of the **DUT** on **OSA**.

Note:

- Set the **OSA** to work in vacuum mode before reading the result.
- The wavelength scanning range of the **OSA** is advised to be set at 20 nm, and the wavelength scanning accuracy is advised to be set at 0.02 nm.

f When for a multi-lane optical module, repeat the test for other lanes.

6.6 RMS Spectral Width

6.6.1 Definition

The **'RMS spectral width'** is a dedicated parameter of the multi-longitudinal mode laser. The unit is nm. It is calculated based on all longitudinal modes with peak power drops of less than 20dB. Figure 6-7 shows the test principles. Use Equation 6-1 and Equation 6-2 for calculation.

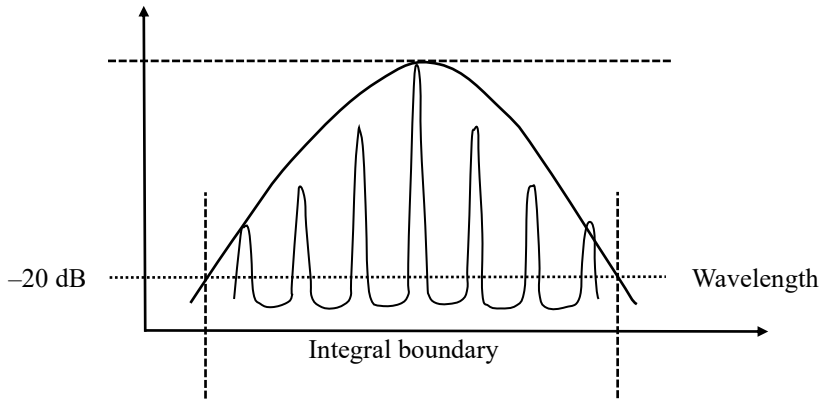


Figure 6-7 RMS spectral width test principles

Equation 6-1: $$\Delta\lambda_{RMS} = \left[\frac{\Sigma P_i \times (\lambda_i - \lambda_c)^2}{\Sigma P_i}\right]^{\frac{1}{2}}$$

Equation 6-2: $$\lambda_c = \frac{\Sigma P_i \times \lambda_i}{\Sigma P_i}$$

Where:

$\Delta\lambda_{RMS}$: the **'RMS spectral width'**

λ_i: wavelength of the *i*th longitudinal mode

P_i: power of the *i*th longitudinal mode

6.6.2 Block Diagram

Figure 6-8 RMS spectral width test

6.6.3 Test Steps

a Connect the test system according to Figure 6-8.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Set the threshold and k value for the **OSA**.

Note: The threshold of the **OSA** is advised to be set at 20.00dB and k is advised to be set at 2.00.

e Read the spectral width Δλ on the **OSA**. The **'RMS spectral width'** is Δλ divided by 2.

f When for a multi-lane optical module, repeat the test for other lanes.

6.7 Average Optical Power(AOP)

6.7.1 Definition

The **'average optical power'** is defined as the average value of the output optical power of each lane at the transmit end under specific working conditions. The unit is dBm.

6.7.2 Block Diagram

Figure 6-9 Average launch optical power test

6.7.3 Test Steps

a Connect the test system according to Figure 6-9.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Read the **'average optical power'** on the **Optical power meter**.

e When for a multi-lane optical module, repeat the test for other lanes.

6.8 Outer Optical Modulation Amplitude (OMA_{outer})

6.8.1 Definition

The **'outer optical modulation amplitude'** of PAM4 signal is defined as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 6-10. The unit is dBm.

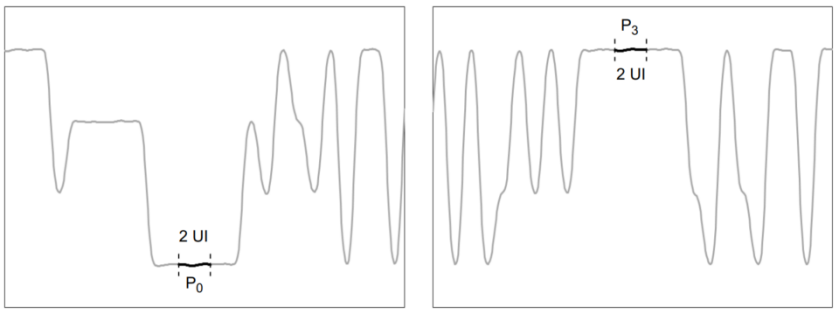


Figure 6-10 Example power levels P_0 and P_3 from PRBS13Q test pattern

OMA_{outer} can be written mathematically as:

Equation 6-3: $OMA_{outer} = P_3 - P_0$

Equation 6-4: $P_{mean} = (P_3 + P_0)/2$

Equation 6-5: ER=P3/P0

Through algebraic manipulation of Equations 6-3, 6-4 and 6-5, the following relationship can be obtained:

Equation 6-6: $OMA_{outer} = 2 \times P_{mean} \times (ER_{outer} - 1)/(ER_{outer} + 1)$

Where:

P_3 is the average value of 2 UI in the middle of 7 consecutive 3-level bits, the unit is W.

P_0 is the average value of 2 UI in the middle of 6 consecutive 0-level bits, the unit is W.

P_{mean} is close to the mean of the light levels for " 3-level" and "0-level ", the unit is W.

ER_{outer} is the extinction ratio, the unit is dB.

6.8.2 Test Steps

a Record the **'average optical power'** value of each lane by referencing to 6.7.

b Record the '**extinction ratio**' value of each lane by referencing to 6.14.

c Calculate the **'OMA_{outer}'** according to Equation 6-6.

6.9 Launch Power in OMA minus TDECQ, each lane (Min)

6.9.1 Definition

The '**launch power in OMA minus TDECQ, each lane (Min)**'is the minimum value of the launch optical power in the OMA_{outer} minus TDECQ. It can be used to calculate the power budget of an optical module. The unit is dBm.

6.9.2 Test Steps

a Record the **'OMA_{outer}'** value of each lane by referencing 6.8.

b Record the '**TDECQ**' value of each lane by referencing 6.10.

c Calculate the **'launch power in OMA minus TDECQ, each lane (Min)'** according to **6.9.1**.

6.10 Transmitter and Dispersion Eye Closure for PAM4 (TDECQ)

6.10.1 Definition

The '**TDECQ**' is a measure of each optical transmitter's vertical eye closure when transmitted through a worst case optical channel (specified in *IEEE 802.3-2018 121.8.5.2*), as measured through an optical to electrical converter (O/E) and oscilloscope with the combined frequency response given in *IEEE 802.3-2018 121.8.5.1*, and equalized with the reference equalizer (as described in *IEEE 802.3-2018 121.8.5.4*). The reference receiver and equalizer may be implemented in software or may be part of an oscilloscope.

6.10.2 Block Diagram

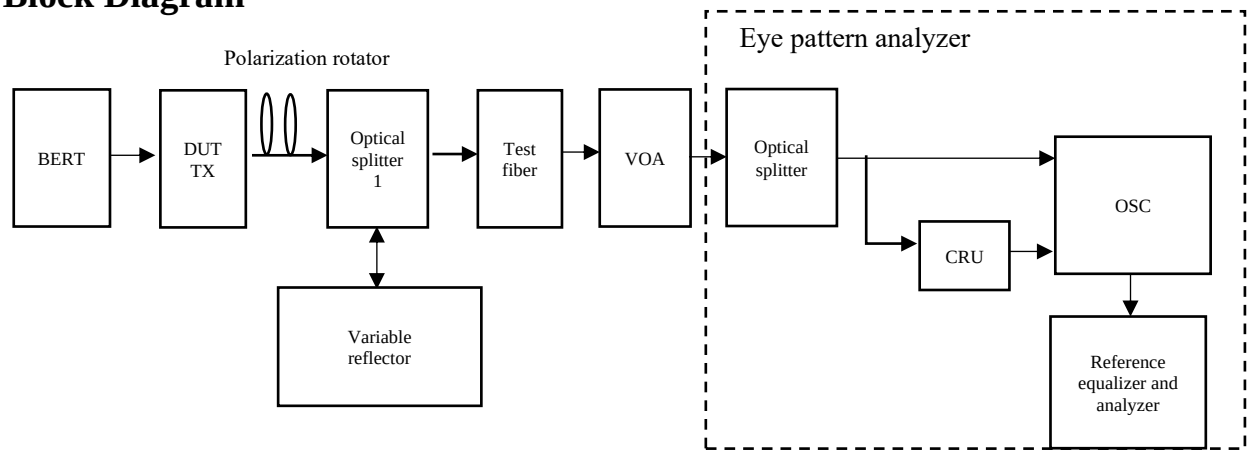


Figure 6-11 TDECQ test

6.10.3 Test Steps

a Connect the test system according to Figure 6-11. Other equivalent measurement implementations may be used with suitable calibration.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Adjust the **Optical splitter 1** and **Variable reflector** to ensure that the transmitter of each lane is tested with compliant optical return loss. The state of **Polarization** of the back reflection is adjusted to create the greatest RIN.

e Ensure that **Test fiber** and **Optical attenuators** meet the specified requirements.

Note:

- The length of the **Test fiber** is advised to be set at 3m.
- The Test fiber should meet the requirements in the protocol, as described in the Table 6-3.

Table 6-3 Transmitter compliance channel specifications

PMD type	**Dispersion[a] (ps/nm)**		**Insertion loss[b]**	**Optical return loss[c]**	**Max mean DGD**
	Minimun	**Maximum**			
100GBASE-DR	$0.011625\times\lambda\times[1-(1324/\lambda)^4]$	$0.011625\times\lambda\times[1-(1300/\lambda)^4]$	Minimum	15.5 dB	0.5ps
100GBASE-FR1	$0.046\times\lambda\times[1-(1324/\lambda)^4]$	$0.046\times\lambda\times[1-(1300/\lambda)^4]$	Minimum	17.1dB	0.8ps
100GBASE-LR1	$0.230\times\lambda\times[1-(1324/\lambda)^4]$	$0.230\times\lambda\times[1-(1300/\lambda)^4]$	Minimum	15.6dB	0.8ps
400GBASE-FR4	$0.046\times\lambda\times[1-(1324/\lambda)^4]$	$0.046\times\lambda\times[1-(1300/\lambda)^4]$	Minimum	17.1dB	0.8ps
400GBASE-LR4-6	$0.138\times\lambda\times[1-(1324/\lambda)^4]$	$0.138\times\lambda\times[1-(1300/\lambda)^4]$	Minimum	15.6dB	0.8ps

f Read the '**TDECQ**' on **Eye pattern analyzer.**

Note:

- Configure the pattern-triggered Oscillograph **(OSC)** to capture the complete pattern for TDECQ analysis. The eye diagram is formed based on **CRU**. TDECQ is given after the equalization with the **Reference equalizer and analyzer**.
- The **Reference equalizer and analyze**r for TDECQ is a 5 tap, T spaced, feed-forward equalizer (FFE), where T is the symbol period. The sum of the equalizer tap coefficients is 1(*Defined in IEEE 802.3-2018 121.8.5.4*).
- The combination of the O/E and the OSC has a fourth-order Bessel-Thomson filter response with a bandwidth of approximately 13.28125GHz. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

- The test pattern (specified in Table 6-2) is transmitted repetitively by the optical lane under test and the OSC is set up to capture the complete pattern for TDECQ analysis as described in *IEEE 802.3-2018 121.8.5.3*. The CRU has a corner frequency of 4MHz and a slope of 20dB/decade. The CRU can be implemented in hardware or software depending on OSC technology.

g When for a multi-lane optical module, repeat the test for other lanes.

6.11 TDECQ Minus 10 $\log_{10}$(Ceq)

6.11.1 Definition

Ceq is a coefficient which accounts for the reference equalizer noise enhancement. The value of Ceq can be calculated from the product of the normalized noise power density spectrum N(f) at the input of the reference equalizer and the normalized frequency response Heq(f) of the reference equalizer, as shown in Equation 6-7. The '**TDECQ Minus 10 log10(Ceq)**' is calculated according to Equation 6-8.

Equation 6-7: $\mathrm{Ceq} = \sqrt{\int_f \mathrm{N}(f) \times |\mathrm{Heq}(f)|^2 \mathrm{d}f}$

Where:

N(f) is the normalized noise power density spectrum equivalent to white noise filtered by a fourth order Bessel-Thomson response filter with a bandwidth of 26.5625GHz.

$\int_f \mathrm{N}(f)df = \mathrm{Heq}(f{=}0) = 1$

Equation 6-8: $Tm = T - 10 * log_{10}^{C}$

Where:

Tm is '**TDECQ Minus 10 log10(Ceq)**', the unit is dB.

T is TDECQ of the optical module, the unit is dB.

C is a coefficient which accounts for the reference equalizer noise enhancement.

6.11.2 Block Diagram

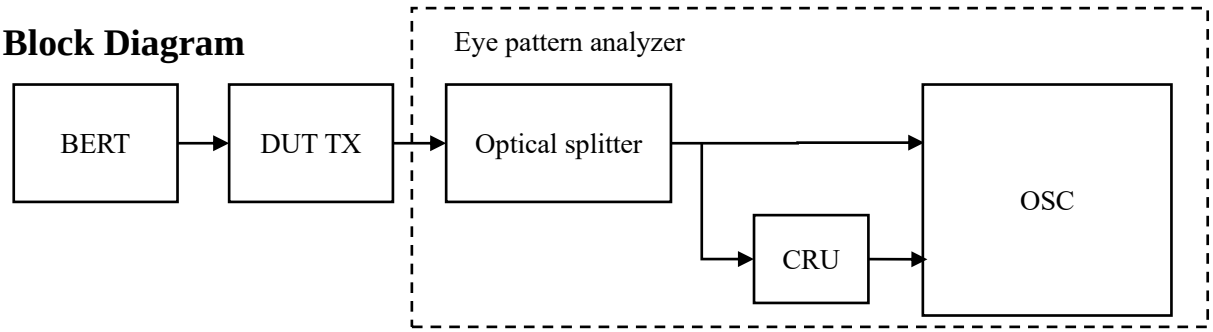


Figure 6-12 Ceq test

6.11.3 Test Steps

a Connect the test system according to Figure 6-12.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Read the Ceq on the **OSC.**

e Calculate the '**TDECQ Minus 10 log10(Ceq)**' according to Equation 6-8.

f When for a multi-lane optical module, repeat the test for other lanes.

6.12 Average Launch Power of OFF Transmitter

6.12.1 Definition

The **'average launch power of OFF transmitter'** is the output optical power after the laser of a single lane is shut down.

6.12.2 Block Diagram

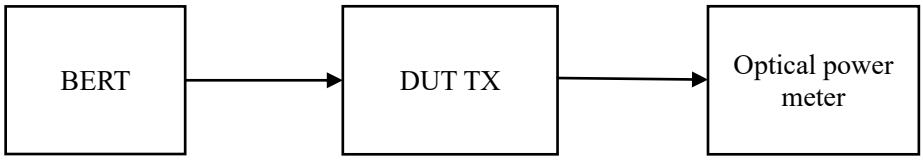


Figure 6-13 Average launch power of off transmitter test

6.12.3 Test Steps

a Connect the test system according to Figure 6-13.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Configure the protocol register of the **DUT** to disable the transmit optical power of the lane under test.

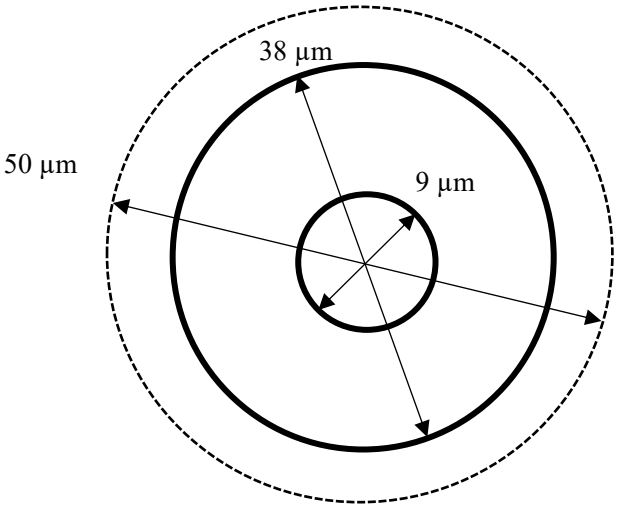
e Read the '**average launch power of OFF transmitter'** on the **Optical power meter**.

f When for a multi-lane optical module, repeat the test for other lanes.

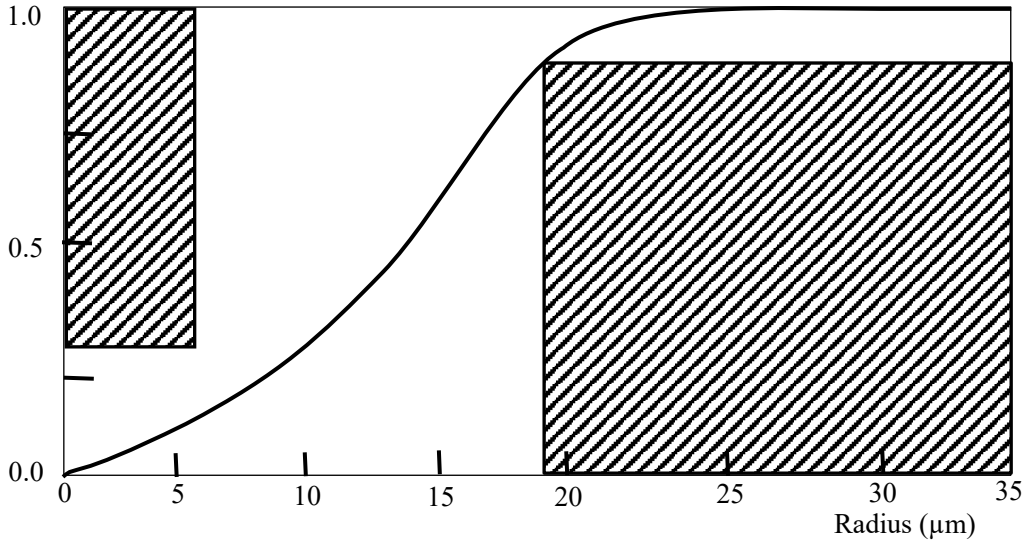
6.13 Encircled Flux(EF)

6.13.1 Definition

The near-field light intensity of the circular beam emitted by a vertical-cavity surface-emitting laser (VCSEL) is in the shape of a donut, and the central light intensity of the fiber core is approximately zero. This laser emission output feature is called '**Encircled Flux (EF)**'. The encircled flux at 19 m shall be greater than or equal to 86% and the encircled flux at 4.5 m shall be less than or equal to 30% when measured into 50/125 um multimode fiber. Figure 6-14(a) shows intensity distribution diagram of VCSEL light spot. Figure 6-14(b) shows Encircled Flux specification.



(a) Radial energy distribution diagram of VCSEL light spot



(b) Encircled Flux specification

Figure 6-14 Encircled flux test principles

6.13.2 Block Diagram

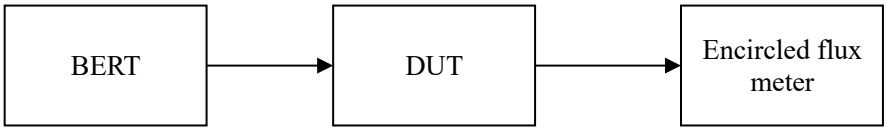


Figure 6-15 Encircled flux test

6.13.3 Test Steps

a Connect the test system according to Figure 6-15.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested by turning on only one laser under test or by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Read the '**EF**' on the **Encircled flux meter.**

Note: The test is advised to cover the 19 μm and 4.5 μm diameter points.

e When for a multi-lane optical module, repeat the test for other lanes.

6.14 Extinction Ratio(ER)

6.14.1 Definition

The '**extinction ratio**' of PAM4 signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 6-16.

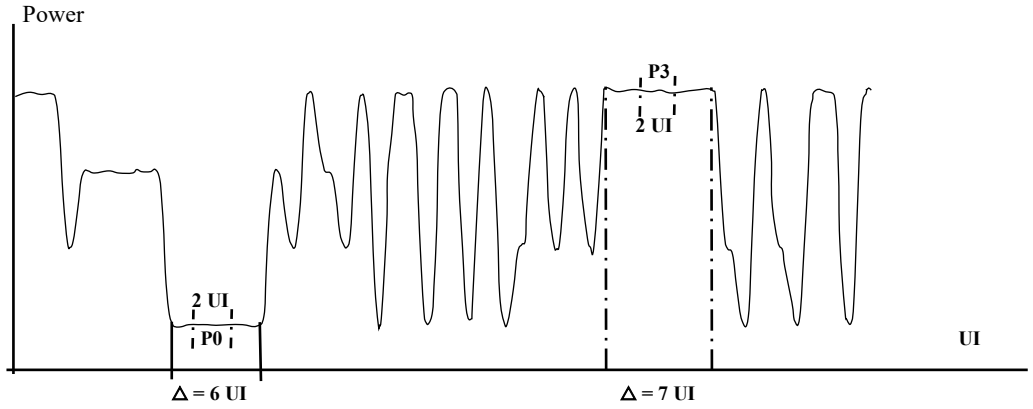


Figure 6-16 Example power levels P_0 and P_3 from PRBS13Q test pattern

6.14.2 Block Diagram

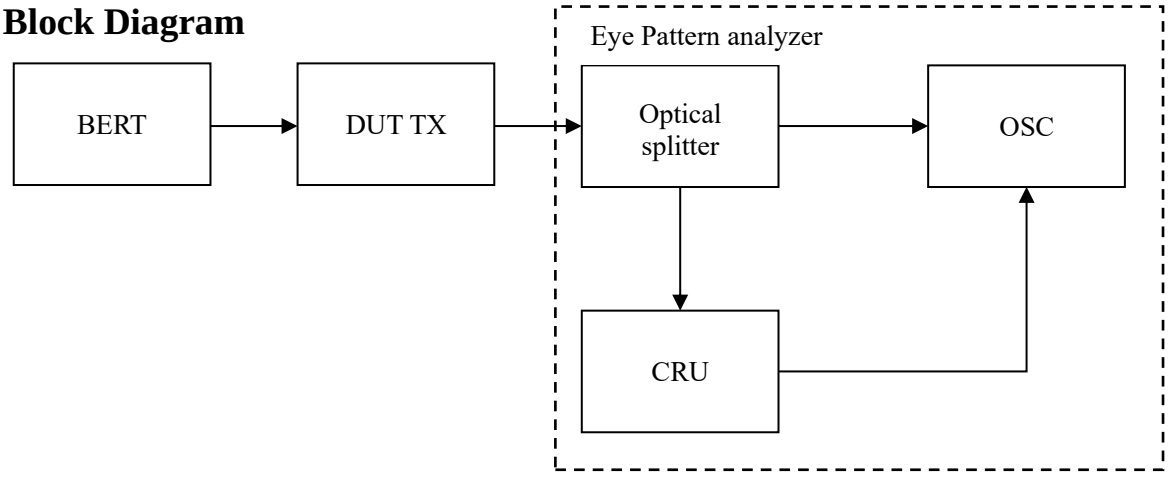


Figure 6-17 Extinction ratio test

6.14.3 Test Steps

a Connect the test system according to Figure 6-17.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested by turning on only one laser under test or by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Read the '**ER**' on the **Eye pattern analyzer**.

Note:

- Perform **OSC** dark current calibration and enable pattern lock before reading the result.

e When for a multi-lane optical module, repeat the test for other lanes.

6.15 Transmitter Transition Time

6.15.1 Definition

The '**transmitter transition time**' is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer} or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling time respectively, as measured through an O/E converter and oscilloscope with response defined as follows. The combined response of the O/E converter and oscilloscope has a 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz. At frequencies above 1.3 × 53.125 GHz the response should not exceed –20dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response. The unit is ms.

The 0% level and the 100% level are P0 and P3as defined by the OMAouter measurement procedure (see IEEE 802.3cu-2021 151.8.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence.

6.15.2 Block Diagram

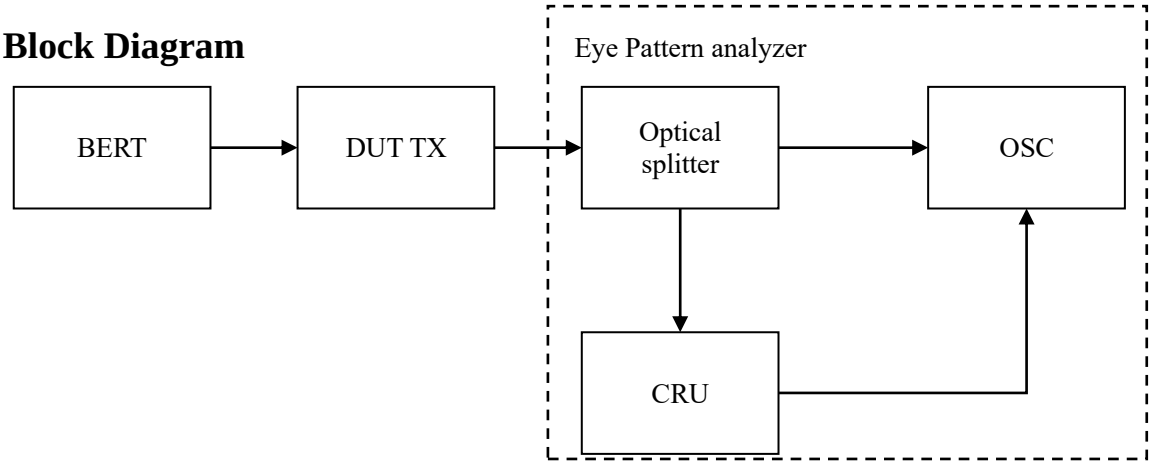


Figure 6-18 Transmitter transition time test

6.15.3 Test Steps

a Connect the test system according to Figure 6-18.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested by turning on only one laser under test or by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Read the rising time and falling time on the **OSC**.

Note:

- Enable pattern lock before reading.
- The **CRU** has a corner frequency of 4 MHz and a slope of 20 dB/decade. The combination of the O/E and the oscilloscope has a fourth-order Bessel-Thomson filter response with a bandwidth of approximately 26.5625 GHz.

e When for a multi-lane optical module, repeat the test for other lanes.

6.16 RIN_xOMA

6.16.1 Definition

The '**relative intensity noise optical modulation amplitude (RIN_xOMA)**' represents the distribution of 3-level and 0-level noise of the laser output optical signal relative to optical modulation amplitude in the specified bandwidth under the specified reflected optical power, show in Equation 6-9. The unit is dB/Hz.

Equation 6-9： $RIN_xOMA = 10lg(RN_{three}+RN_{zero})/(OMA\times BW)$

RIN_xOMA: relative intensity noise optical modulation amplitude in dB/Hz.

RN_{three} : 3-level random noise power in W.

RN_{zero} : 0-level random noise power in W.

OMA : optical modulation amplitude in W.

BW : bandwidth of low-pass filter in Hz.

6.16.2 Block Diagram

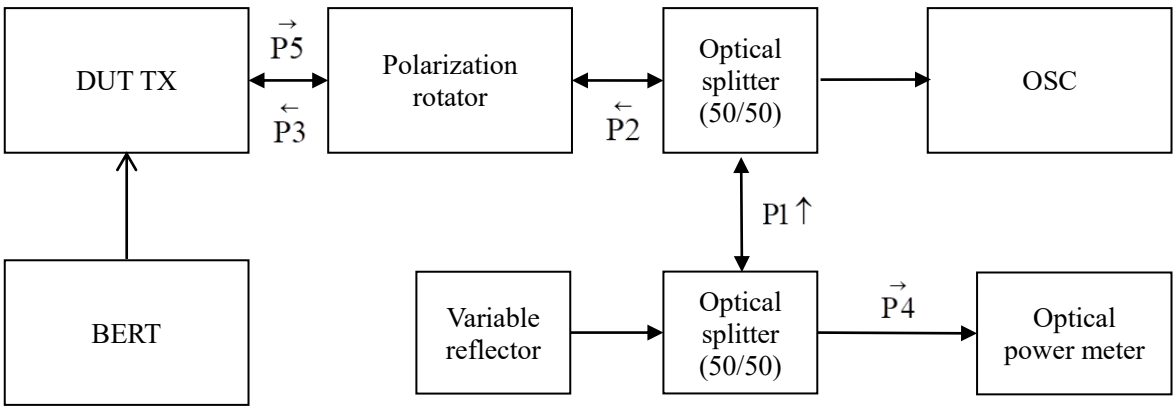


Figure 6-19 RIN_xOMA test

6.16.3 Test Steps

a Connect the test system according to Figure 6-19.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c Adjust the **VOA**. Test P1, P2, P3, P4, P5 defined in Figure 6-19 using the **Optical power meter**.

d Calculate as follows: ΔP1 = P1 – P4, ΔP2 = P2 – P1, ΔP3 = P3 – P2. Then, calculate the reflected optical power as follows: Pr = P4 + ΔP1 + ΔP2 + ΔP3, x = |Pr – P5|, x should meet return loss of the specification.

e Don't let the optical power of the **DUT** enter the **OSC.** Enable the **OSC** optical port, use a histogram to collect the background noise of the **OSC** optical port, measure the RMS random noise power, obtain the standard deviation, and set the noise test result compensation value.

Note: The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 53.125 GHz).

f When for a multi-lane optical module, ensure that each optical lane is tested individually by turning on only one laser under test or by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

g Let the optical power of the DUT enter **OSC** optical port through a short optical fiber patch cord (< 2 m). Use the **OSC** to measure the 3-level random noise power (RN_{three}) and the 0-level random noise power (RN_{zero}) of the DUT optical eye.

h Measure the optical modulation amplitude.

i Calculate RIN_xOMA according to Equation 6-9.

j When for a multi-lane optical module, repeat the test for other lanes.

6.17 Transmitter Reflectance (Max)

6.17.1 Definition

The '**transmitter reflectance**' is defined as the ratio of reflected power to incident power input into the transmitter. The unit is dB.

6.17.2 Block Diagram

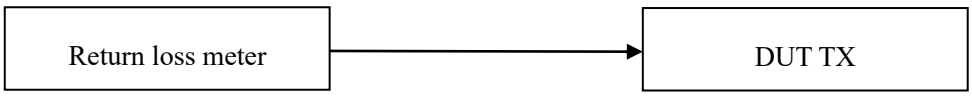


Figure 6-20 Transmitter reflectance test

6.17.3 Test Steps

a Connect the test system according to Figure 6-20.

b Set the wavelength of the **Return loss meter** to the working wavelength of the optical module.

c Cover the end face of the test optical fiber connected to the **Return loss meter**.

d Use the method of external calibration return loss meter for calibration.

e After the calibration, save the calibration parameters and connect the optical fiber to the test end face.

f Read the value on the **Return loss meter** and record it as transmitter reflectance.

6.18 Optical Return Loss Tolerance (Max)

6.18.1 Definition

‘**Optical return loss tolerance (max)**’is the ratio of the **‘average launch power’** to the maximum returned optical power that can be tolerated. The unit is dB.

6.18.2 Block Diagram

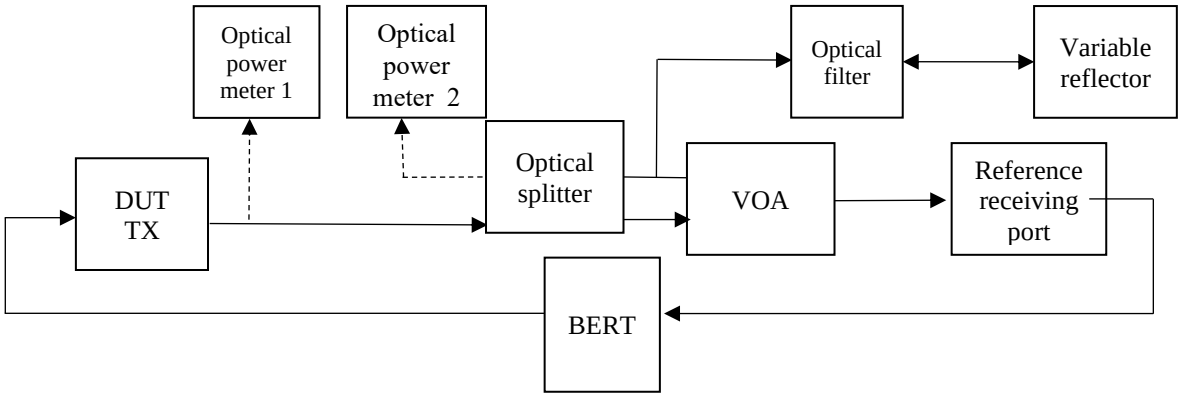


Figure 6-21 Optical return loss tolerance test

6.18.3 Test Steps

a Connect the test system according to Figure 6-21.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Disconnect the variable reflector and terminate the corresponding port. Read the launch optical power P0(the unit is dB) of the optical module on **Optical power meter_1** under error-free condition.

e Adjust the **VOA** to ensure that the optical power entering the **Reference receiving port** is the maximum value of the receiver sensitivity.

f Connect the **Variable reflector** and adjust it to gradually increase the optical reflectance. Measure the reflected power P1 of the optical module on **Optical power meter_2** when bit error occurs. Other parameters (such as ‘**TDECQ**’ and ‘**SMSR**’) also need to meet specifications.

g Calculate the **‘optical return loss tolerance (max)’** as P0-P1.

h When for a multi-lane optical module, repeat the test for other lanes.

6.19 Transfer Delay

6.19.1 Definition

The **‘transfer Delay’** is defined as the maximum delay of data transmission between different layers.

6.19.2 Block Diagram

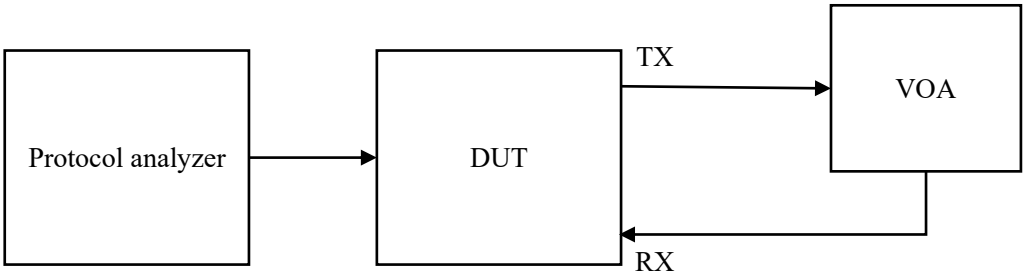


Figure 6-22 Transfer delay test

6.19.3 Test Steps

a Connect the test system according to Figure 6-22.

b Read the delay value T0 on the **Protocol analyzer** without the optical module in self-loop.

c Read the delay value T1 on the **Protocol analyzer** with the optical module in self-loop using a test fiber.

d Calculate the ‘**transfer delay**’ as T1 – T0.

6.20 Difference in Launch Power Between Any Two Lanes (OMA_{outer})

6.20.1 Definition

The ‘**difference in launch power between any two lanes(OMA_{outer})**’ of PAM4 signal is defined as the difference between the maximum and minimum OMA_{outer} values of all lanes in a 400G module. The unit is dB.

6.20.2 Test Steps

a Record the ‘**OMAouter**’ values of all lanes by referencing **6.8**.

b The ‘difference in launch power between any two lanes’ is the maximum ‘**OMA_{outer}**’ of all lanes minus the minimum ‘**OMA_{outer}**’.

6.21 Transmitter Eye Closure for PAM4 (TECQ)

6.21.1 Definition

The ‘t**ransmitter eye closure for PAM4 (TECQ)**’ test measures the quality of an optical module transmitter. **‘TECQ’** is the optical power penalty of the measured optical module transmitter compared with an ideal transmitter. The unit is dB.

The ‘TECQ’ is defined as:

Equation 6-10: $TECQ = 10 \times \lg[OMA_{outer} / (6 \times Q_t \times R)]$

Where:

OMA_{outer}: outer optical modulation amplitude.

Q_t: 3.414, consistent with the target symbol error ratio for Gray coded PAM4.

R: derived from the equation: $R = \sqrt{\sigma_{G2} + \sigma_{S2}}$

σ_S: standard deviation of the noise of the O/E and oscilloscope combination.

σ_G: Gaussian probability density functions centered around the sub-eye thresholds.

6.21.2 Block Diagram

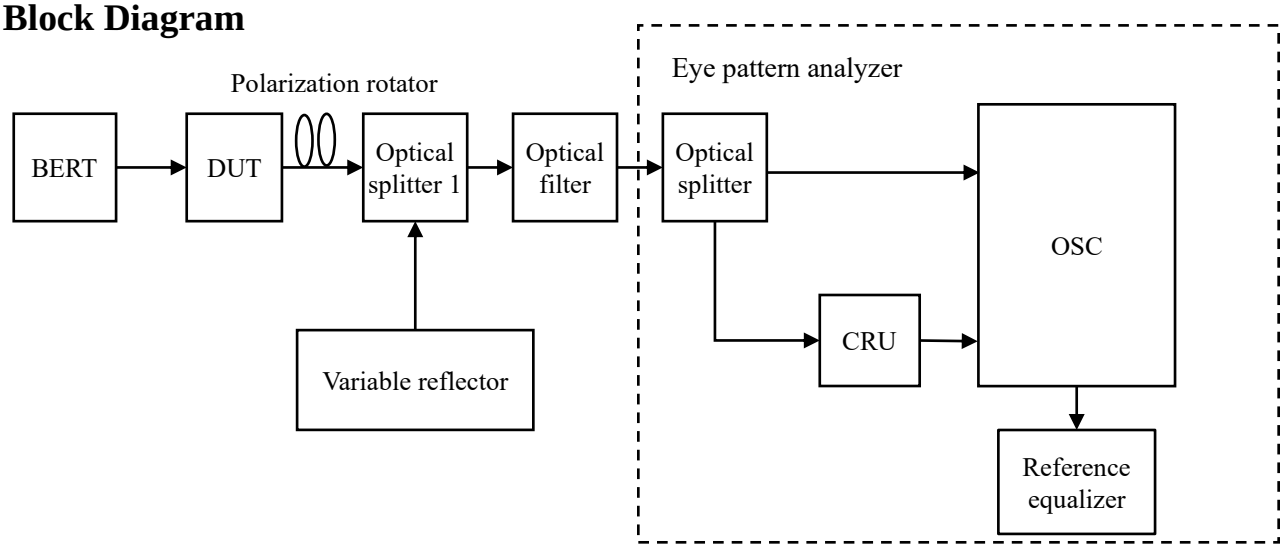


Figure 6-23 TECQ test

6.21.3 Test Steps

a Connect the test system according to Figure 6-23.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Adjust the **Optical splitters 1** and **Variable reflector** to ensure that the transmitter is tested with the specified optical return loss.

e Adjust the state of polarization of the back reflection via **Polarization rotator**.

f Read the '**TECQ**' value on the **Eye pattern analyzer**.

Note:

- The **CRU** has a corner frequency of 4 MHz and a slope of 20 dB/decade.
- Select the bandwidth with a fourth-order Bessel-Thomson filter response specified for the module test.

- Configure the **OSC** to capture the complete pattern before reading the result.

g When for a multi-lane optical module, repeat the test for other lanes.

6.22 |TDECQ – TECQ| (Max)

6.22.1 Definition

The **'|TDECQ – TECQ| (Max)'**is defined as the maximum absolute difference between the TDECQ value and TECQ value among four lanes. It can be used to measure the dispersion penalty of optical transmission on a link.

6.22.2 Test Steps

a Record the '**TDECQ**' values of each lane by referencing 6.10**.**

b Record the '**TECQ**' values of each lane by referencing 6.21**.**

c The **'|TDECQ – TECQ| (Max)'** is the maximum of the absolute difference between the '**TDECQ**' value and '**TECQ**' value of each lane.

6.23 Over/undershoot

6.23.1 Definition

The '**overshoot'** is defined as the maximum power above the 3-level power relative to '**OMA_{outer}**', calculated as Equation 6-11.The unit is %.

Equation 6-11: $Overshoot = (P_{max} - P_3)/OMA_{outer} \times 100$

The '**undershoot'** is defined as the minimum power from the transmitter (P_{min}) below the 0-level power relative to the **'OMA_{outer}',** calculated as Equation 6-12.The unit is %.

Equation 6-12: $Undershoot = (P_0 - P_{min})/OMA_{outer} \times 100$

Where:

P_{max} : is based on a 10^{-2} hit ratio, where P_{max} is the smallest power level that results in the number of samples above that level not exceeding the product of the hit ratio and total number of observed samples, with all samples acquired in a single unit interval eye diagram.

P_{min} : is based on a 10^{-2} hit ratio, where P_{min} is the largest power level that results in the number of samples below that level not exceeding the product of the hit ratio and total number of observed samples, with all samples acquired in a single unit interval eye diagram.

P_3 : is the power of the PAM4 3-level defined in *IEEE 802.3cu-2021 122.8.4*.

P_0 : is the power of the PAM4 0-level defined in *IEEE 802.3cu-2021 122.8.4*.

OMA_{outer}**:** is the outer optical modulation amplitude defined in *IEEE 802.3cu-2021 122.8.4*.

6.23.2 Block Diagram

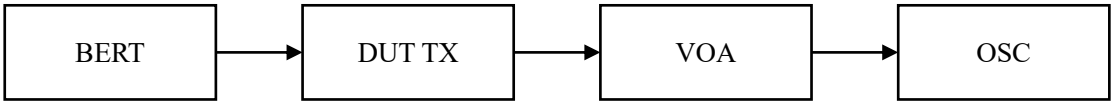


Figure 6-24 Transmitter overshoot/undershoot test

6.23.3 Test Steps

a Connect the test system according to Figure 6-24.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Use the waveform captured for TDECQ test (reference 6.10) and the waveform captured for TECQ test (reference 6.21), but without the reference equalizer being applied in either case. Read the P_{max}, P_{min}, P3 and P0(defined in 6.23.1) on the **OSC**.

e Record the '**OMA_{outer}**' values of each lanes by referencing 6.8.

f Calculate the **'overshoot'** and '**undershoot**' values according to Equation 6-11 and Equation 6-12, respectively.

g When for a multi-lane optical module, repeat the test for other lanes.

6.24 Transmitter Power Excursion

6.24.1 Definition

The **'transmitter power excursion'** is defined as Equation 6-13.The unit is dBm.

Equation 6-13: Transmitter power excursion = max ($P_{max} - P_{average}$, $P_{average} - P_{min}$)

Where:

P_{max} and P_{min} : defined in 6.23.1

$P_{average}$: **'average optical power'** defined in 6.7.

6.24.2 Block Diagram

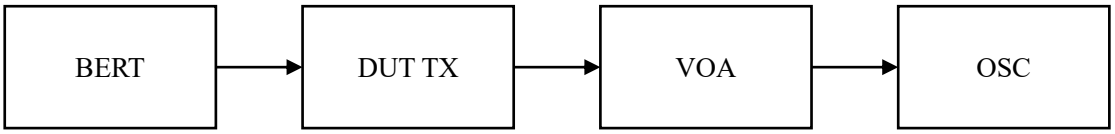


Figure 6-25 Transmitter power excursion test

6.24.3 Test Steps

a Connect the test system according to Figure 6-25.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Use the waveform captured for TDECQ test (reference 6.10) and the waveform captured for TECQ test (reference 6.21), but without the reference equalizer being applied in either case. Read the P_{max}, P_{min}(defined in 6.24.1) on the **OSC**.

e Record the OMA_{outer} values of all lanes by referencing 6.8.

f Calculate the **'transmitter power excursion'** value**s** according to the Equation 6-13.

g When for a multi-lane optical module, repeat the test for other lanes.

6.25 Damage Threshold, Each Lane

6.25.1 Definition

The **'damage threshold'** is defined as the launch optical power level, at which the optical module receiver shall be able to tolerate of continuous exposure without being damaged.

6.25.2 Block Diagram

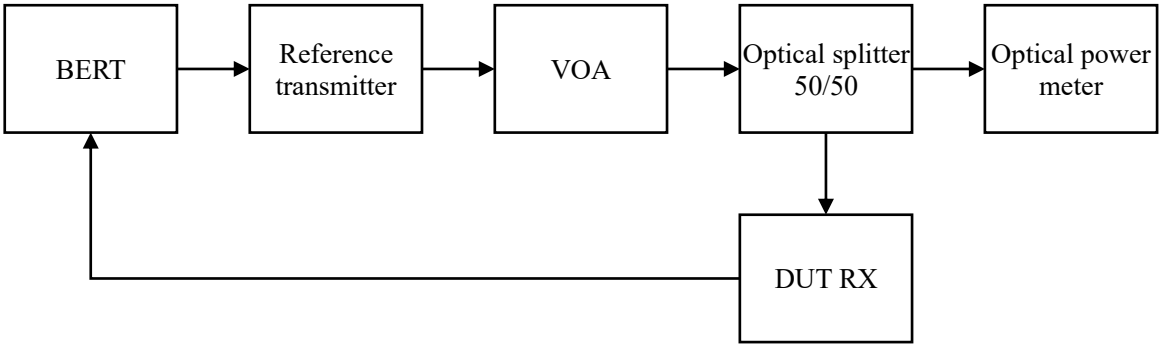


Figure 6-26 Damage threshold test

6.25.3 Test Steps

a Connect the test system according to Figure 6-26.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c Enable all lanes on the multi-lane module and adjust the optical attenuator properly. Ensure that the launch optical power of the **Reference transmitter** is within the normal receiving optical power range of the **DUT**.

d Increase the attenuation of the **VOA**. And record the sensitivity points of each lane.

e Decrease the attenuation of the **VOA** to ensure that the input optical power of each lane reaches the **'damage threshold'** monitored by the **Optical power meter**. And record the BER of each lane.

f Keep the input optical power unchanged for at least 5 minutes. During this period, continuously power on and off the **Reference transmitter**.

g Repeat Steps d to e.

h Verify that the optical indicators of the **DUT** are not degraded after strong light is irradiated.

6.26 Average Receive Power(Max/Min)

6.26.1 Definition

The '**average receive power, each lane (max)**' indicates the overload receive power of each lane. The '**average receive power, each lane (min)**' is informative and not the principal indicator of signal strength. And the receive power below this value is incompliant; however, a value above this does not ensure compliance.

6.26.2 Block Diagram

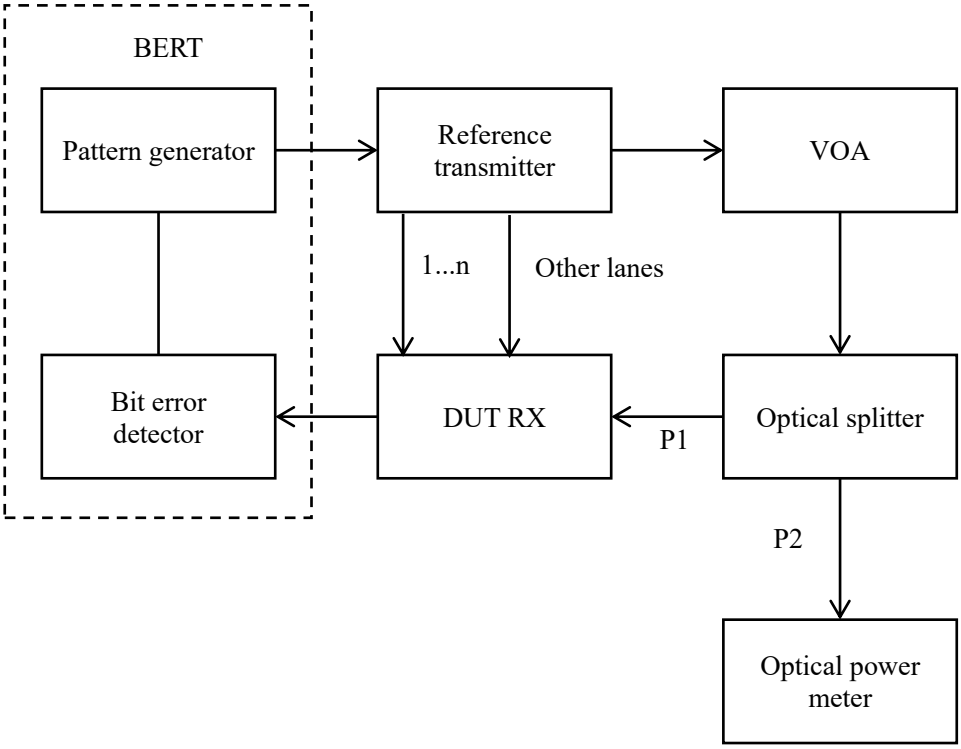


Figure 6-27 Average receive power test

6.26.3 Test Steps

a Connect the test system according to Figure 6-27.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c Set the minimum attenuation value of the **VOA.** Record the P1 and P2(defined in Figure 6 27) of the two output ports of the Optical splitter. And calculate the value: $\Delta P = P2 - P1$. Then the P1 value can be calculated by $P1 = P2 + \Delta P$.

d When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

e Adjust the launch optical power of the **Reference transmitter** output P until P1 is higher than the specified value of '**average receive power, each lane (max)**'. Record the P value at this time and leave it unchanged.

f Adjust the attenuation value of the **VOA** until P1 equals the specified value of '**average receive power, each lane (min)**'.

g Connect the output port of the **Optical splitter** to the DUT. Check whether the receive optical power reported by the DDM of the DUT is normal. Increase the attenuation value of the **VOA** and observe the DDM of **DUT** until the DDM of receive optical power is –40 dBm.

h Gradually reduce the attenuation value of the **VOA** until P1 equals the '**average receive power, each lane (max)**'.

i During attenuation adjustment, check whether the receive optical power reported by the DDM of the **DUT** is normal and record the BER on the **BERT**. Observe whether the BER decreases linearly with the increase of receive optical power, and whether BER abnormally increases near '**the average receive power, each lane (max)**'. Determine whether the BER near the '**average receive power, each lane (max)**' is greater than the specification value.

Note: The SECQ of reference transmitter's optical eye is 0.9 dB (an ideal input signal without overshoot). The test signal should have negligible impairments such as inter-symbol interference (ISI), rise/fall times, jitter and RIN.

6.27 Receive Power (OMA_{outer})

6.27.1 Definition

The '**receive power (OMA_{outer})**' is defined as outer optical modulation amplitude of the receive power per lane. The unit is dBm. Calculate receive power (OMA_{outer}) using Equation 6-14:

$$P_{r(OMA)} = 10 \times \log_{10}\left(2 \times 10^{\frac{P_r}{10}} \times \frac{10^{\frac{ER}{10}} - 1}{10^{\frac{ER}{10}} + 1}\right)$$

Equation 6-14**:**

Where:

$P_{r(OMA)}$: 'receive power(OMA_{outer})'.

P_r: receive power.

ER: 'ER' defined in 6.14.

6.27.2 Block Diagram

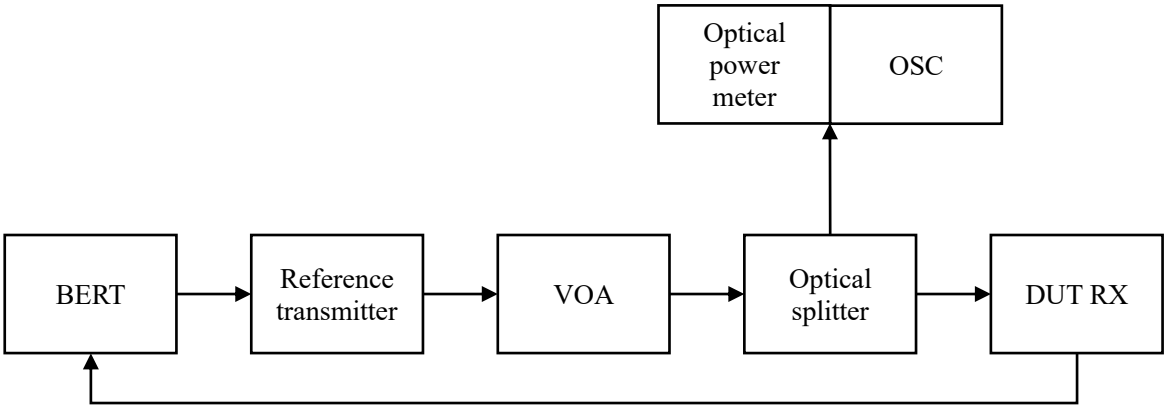


Figure 6-28 Receive power (OMA_{outer}) test

6.27.3 Test Steps

a Connect the test system according to Figure 6-28.

b When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

c Adjust the launch optical power of the **Reference transmitter** and record the receive power (P_r) of each lane.

d Record the '**ER**' value of each lane by referencing 6.14.

e Calculate the '**receive power (OMAouter)**' using Equation 6-14.

f When for a multi-lane optical module, repeat the test for other lanes.

Note: The SECQ of **Reference transmitter**'s optical eye is 0.9 dB (an ideal input signal without overshoot). The test signal should have negligible impairments such as inter-symbol interference (ISI), rise/fall times, jitter and RIN.

6.28 Receiver Reflectance

6.28.1 Definition

The **'receiver reflectance'** is the ratio of the incident optical power to the total returned optical power from the optical module receiver. The unit is dB.

6.28.2 Block Diagram

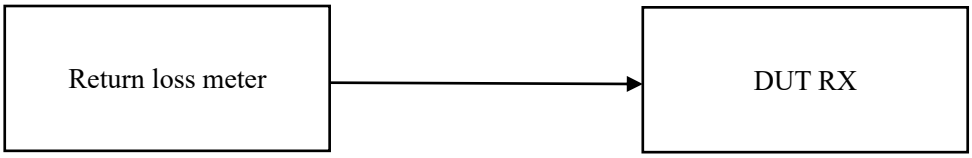


Figure 6-29 Receiver reflectance test

6.28.3 Test Steps

a Connect the test system according to Figure 6-29.

b Turn off the power supply of the **DUT** and set the transmit wavelength of the **Return loss meter** to a value within the working wavelength range of the optical module.

Note: The light source of the **Return loss meter** should support tunable multi-wavelength

c Read the '**reflection coefficient**' value on the **Return loss meter**.

Note: If the transmit wavelength of the **Return loss meter** cannot be set to a value within the working wavelength range of the optical module, use the circulator method.

6.29 Receiver Sensitivity (OMA_{outer})

6.29.1 Definition

The receiver sensitivity is defined as the minimum average optical power per lane when the specified BER of the optical module is met at the specified modulation rate. The unit is dBm.

The '**receiver sensitivity (OMA$_{outer}$)**' is defined as optical modulation amplitude of the receiver sensitivity. The unit is dBm.

6.29.2 Block Diagram

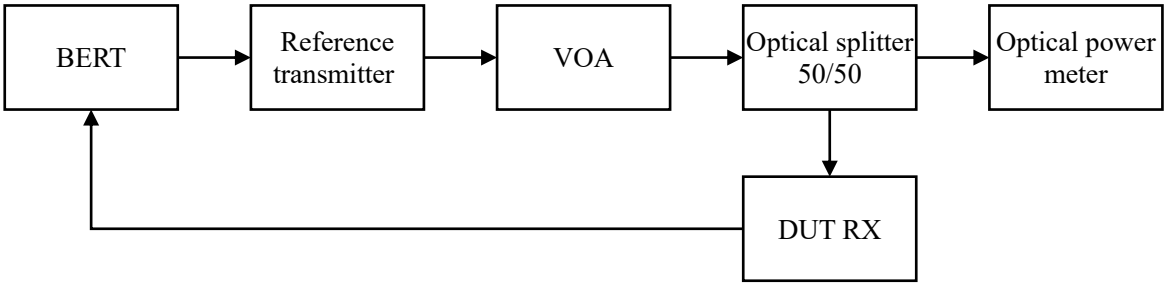


Figure 6-30 Receiver sensitivity test

6.29.3 Test Steps

a Connect the test system according to Figure 6-30.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by turning on only one laser under test or by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Adjust the attenuation value of the **VOA** to gradually reduce the optical power received by the **DUT**, until the BER detected by **BERT** increases to the specified value.

Note: The step of adjusting the VOA is advised to be set at 0.5dB until the measured BER is around BER 1E-6. The step of adjusting the VOA is advised to be set at 0.1dB until the measured BER rests stably at 2.4E-4.

e Read the optical power value on the **Optical power meter**. The value is the receiver sensitivity.

f Record the '**ER**' of each lane by referencing 6.14.

g Calculate the '**Receiver sensitivity (OMA$_{outer}$)**' according to Equation 6-14.

h When for a multi-lane optical module, repeat the test for other lanes.

Note:

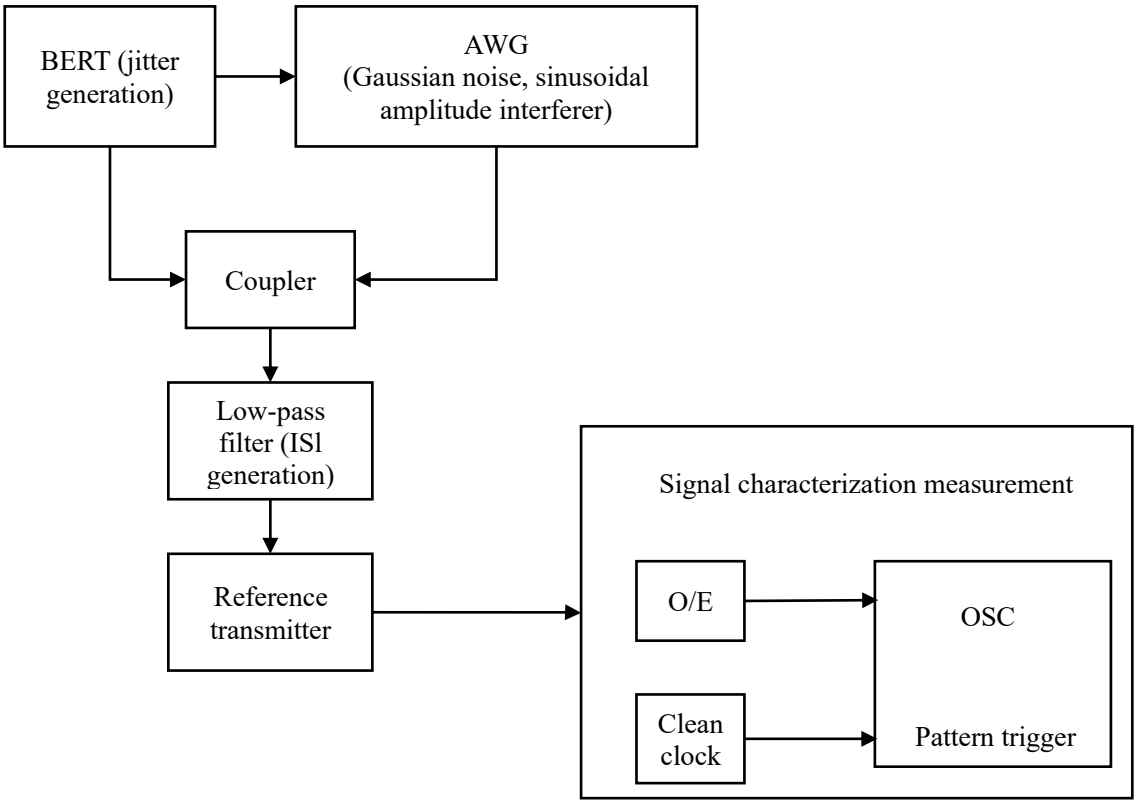
1. The SECQ of **Reference transmitter's** optical eye is 0.9 dB (an ideal input signal without overshoot). The test signal should have negligible impairments such as inter-symbol interference (ISI), rise/fall times, jitter and RIN.

6.30 Stressed Receiver Sensitivity

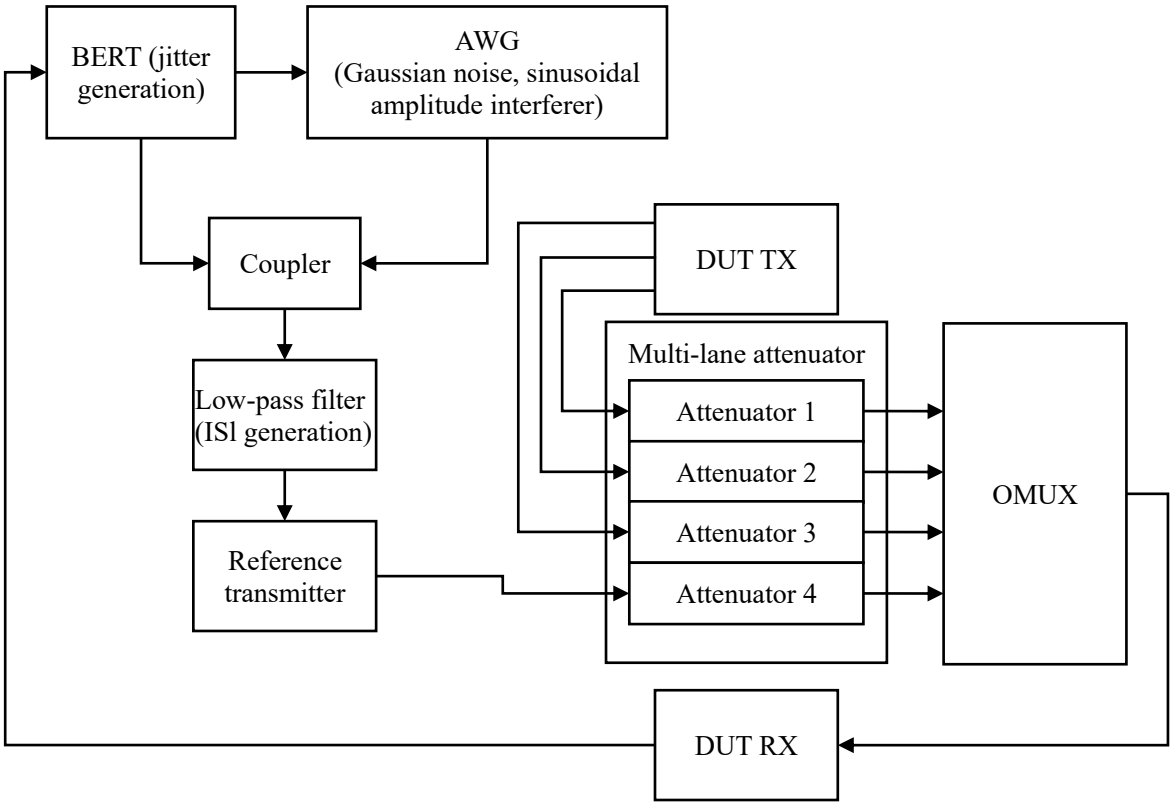
6.30.1 Definition

Under specified pressurization conditions, the **'stressed receiver sensitivity'** is defined as the minimum average optical power per lane when the specified BER of the optical module is met at the specified modulation rate. The unit is dBm.

6.30.2 Block Diagram



(a) Stressed eye calibration test



(b) Stressed receiver sensitivity test

Figure 6-31 Stressed receiver sensitivity test

6.30.3 Test Steps

a Connect the test system according to Figure 6-31.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c Disable the jitter output of the **BERT**, as well as the noise output and sinusoidal interference of the AWG. Set parameters for the external modulator and light source (including adjusting the optical power and configuring the modulator operating point). Test the optical eye pattern of the optical signals output by the modulator. Ensure that the ER value of the optical eye pattern meets the minimum value defined by the protocol. (For details, see the specific requirements in each protocol). Note that polarization maintaining optical fibers must be used for the external modulator and light source.

d Calibrate the SECQ value. Note that the SECQ test method is the same as the TDECQ test method except that the test fiber is removed. During the calibration, if no interference or jitter is added, use the low-pass filter with adjustable cut-off frequency to generate one half of SECQ, and adjust the sinusoidal interference, sinusoidal jitter, and Gaussian noise on the **BERT** and **AWG** to generate the other half of SECQ. The peak-to-peak (UI) and the frequency range of sinusoidal jitter should meet the requirements in the protocol, as described in the following table.

Table 6-4 Applied sinusoidal jitter

Frequency Range	**Sinusoidal Jitter, Peak-to-Peak (UI)**
f < 40 kHz	Not specified
40 kHz < f ≤ 4 MHz	$2 \times 10^5/f$
4 MHz < f < 10 *LB*[a]	0.05

[a] *LB* = loop bandwidth: upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested

Sinusoidal interference and Gaussian noise are not specified in the protocol. You can set them based on the site requirements.

a Ensure that the parameters (ER, SECQ, and OMA) of the optical stressed eye meet the protocol requirements.

b Replace the eye pattern analyzer system with the stressed receiver sensitivity system, as shown in Figure 6-30(b). Retain the parameter adjustment in stressed eye calibration and change the test modulation format to PRBS31Q.

c Perform the stressed receiver sensitivity test according to Figure 6-31. For a single-lane module, OMUX and ODMUX can be removed.

6.31 Receive Overload Power (Average Power)

6.31.1 Definition

The '**receive overload power (Average Power)**' refers to the maximum average optical power that the receiver can receive when the specified BER conditions are met. The unit is dBm.

6.31.2 Block Diagram

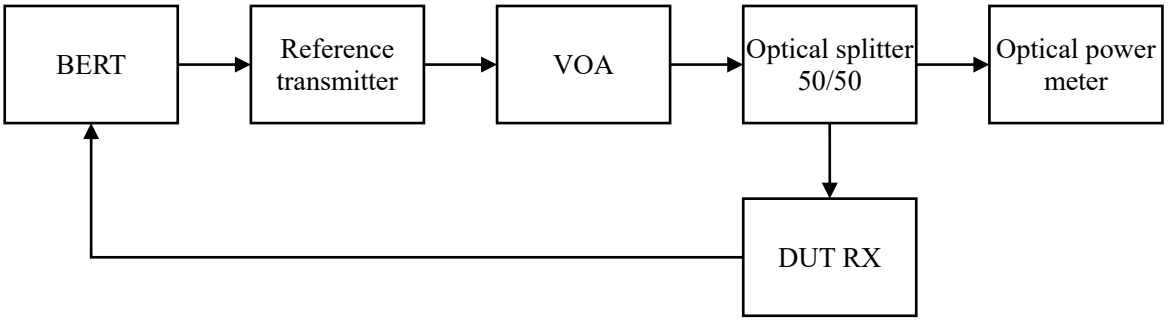


Figure 6-32 Receive power (average power) test

6.31.3 Test Steps

a Connect the test system according to Figure 6-32.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Adjust the attenuation value of the **VOA** to ensure that the input optical power of each lane reaches the maximum receive average power. Record the BER of each lane currently. Compare the recorded BER with the specifications.

e When for a multi-lane optical module, repeat the test for other lanes.

6.32 Receive Overload Power (OMA_{outer})

6.32.1 Definition

The '**receive overload power (OMA_{outer})**' refers to the maximum outer optical modulation amplitude that a receiver can receive when the specified BER conditions are met.

6.32.2 Block Diagram

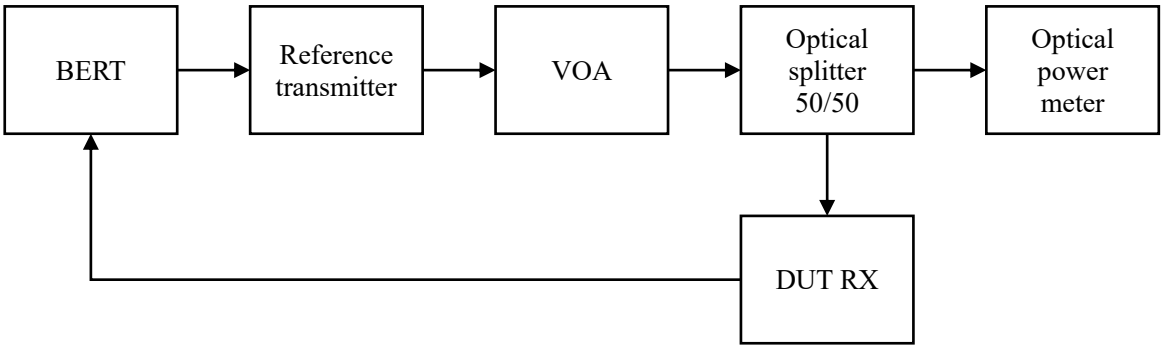


Figure 6-33 Test of receive power (OMA_{outer}) - overload (max)

6.32.3 Test Steps

a Connect the test system according to Figure 6-33.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Adjust the attenuation value of the **VOA** to ensure that the input optical power of each lane reaches the specified maximum receive OMA_{outer} power. Record the BER of each lane currently.

e When for a multi-lane optical module, repeat the test for other lanes.

6.33 Maximum Skew

6.33.1 Definition

The '**maximum skew**' (or relative delay) is defined as the maximum difference between the times of the earliest PCS lane and latest PCS lane for the one-to-zero transition of the alignment marker sync bits.

6.33.2 Block Diagram

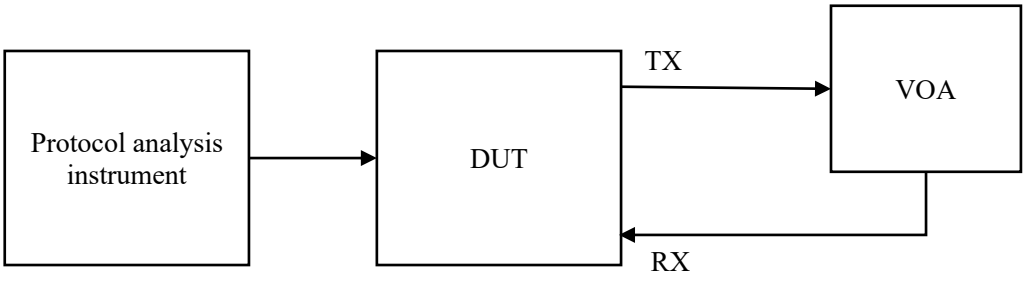


Figure 6-34 Maximum skew test

6.33.3 Test Steps

a Connect the test system according to Figure 6-34.

b Configure the matched service on **Protocol analysis instrument** for the measured optical module and adjust the attenuation value of the **VOA** to ensure that the module works properly.

c Before testing, a calibration of the instrument skew is a need.

d Select **PCS Layer** in the service table. Click **Rx Lane Skew** to read and record the difference between the maximum lane and the minimum lane. The difference is the **'maximum skew'**.

6.34 Maximum Skew Variation

6.34.1 Definition

The skew variation may be introduced due to variations in electrical, thermal, or environmental characteristics. The **'maximum skew variation'** is defined as the maximum change in skew between any PCS lane and any other PCS lane over the entire time that the link is in operation.

6.34.2 Block Diagram

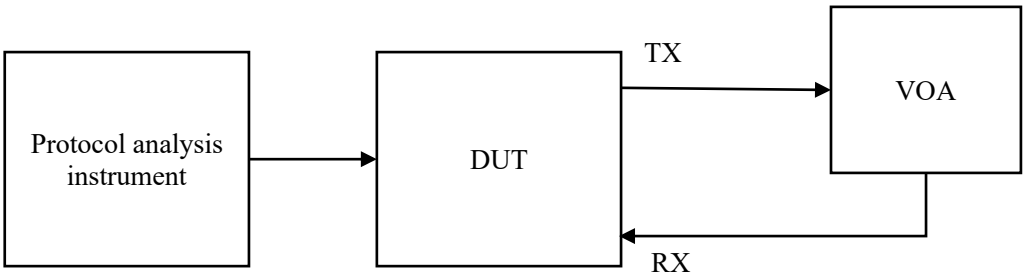


Figure 6-35 Maximum skew variation test

6.34.3 Test Steps

a Connect the test system according to Figure 6-35.

b Configure the matched service on **Protocol analysis instrument** for the **DUT** and adjust the attenuation value of the **VOA** to ensure that the module works properly.

c Select **PCS Layer** in the service table. Click **Rx Lane Skew** to read and record the change value of skew in the same lane.

d Record the skew change values of all lanes in the same way. Select the maximum skew change value and the minimum skew change value for the difference. The difference is the '**maximum skew variation**'.

6.35 Receiver Sensitivity

6.35.1 Definition

The **'receiver sensitivity'** is informative and is defined for a transmitter with a value of SECQ up to 3.4dB. Receiver sensitivity should meet Equation 6-15.

Equation 6-15:RS = max (-6.1, SECQ-7.5) (dB)

Where:

RS: the receiver sensitivity.

SECQ: the SECQ of the transmitter used to measure the receiver sensitivity.

6.35.2 Block Diagram

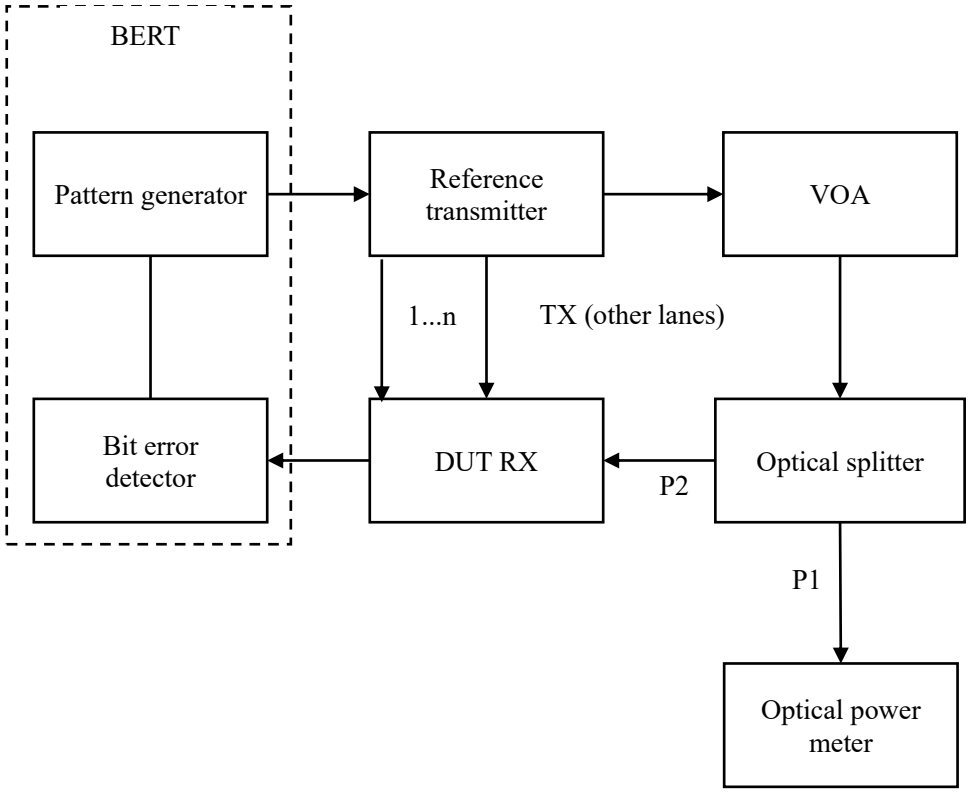


Figure 6-36 Receiver sensitivity test

6.35.3 Test Steps

a Connect the test system according to Figure 6-36.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Measure the optical power values of the two output ports of the splitter to P1 and P2 defined in Figure 6-36, and determine the optical power compensation value using the following equation: ΔP = P2 – P1. Then the receive optical power(P2) of the DUT can be calculated as P2=P1+ΔP.

e Adjust the optical attenuator to 0 dB and wait for a time interval. After confirming the phase lock of the **BERT**, wait until the BER is stable. Then record the BER after 3 seconds.

Note:

Calculate the time interval of error bits accumulation when the is BER tested based on confidence (95%), BER (2.4E-4), and the following equation:

Equation 6-16**:** $CL = 1 - e^{-Nbits \times BER}$

Where:

CL: confidence

N_{bits}: bits accumulation that the pattern generator sends in the time interval.

BER: bit error ratio.

The time interval of error bits accumulation is 2.35E-7s when CL is 95% and the BER is 2.4E-4. The test duration is 3 seconds.

f Adjust the attenuation value of the **VOA** until the measured BER is around BER 1E-6.

Note: The step of adjusting the attenuation value is advised to be set at 0.5dB.

g Adjust the attenuation value of the **VOA** until the measured BER rests stably 2.4E-4.

Note: The step of adjusting the attenuation value is advised to be set at 0.1dB.

h The above receive optical power and the corresponding BER are drawn as a BER curve, according to which the received optical power corresponding to the target BER is obtained, namely, the '**receiver sensitivity**'.

i When for a multi-lane optical module, repeat the test for other lanes.

Note:

The SECQ of the **Reference transmitter**'s optical eye is 0.9 dB (an ideal input signal without overshoot). The test signal should have negligible impairments such as inter-symbol interference (ISI), rise/fall times, jitter and RIN.

6.36 Receiver Sensitivity with Fiber Propagation

6.36.1 Definition

The '**receiver sensitivity with fiber propagation**' is defined as the minimum average receive optical power per lane with fiber propagation when the specified BER is met.

6.36.2 Block Diagram

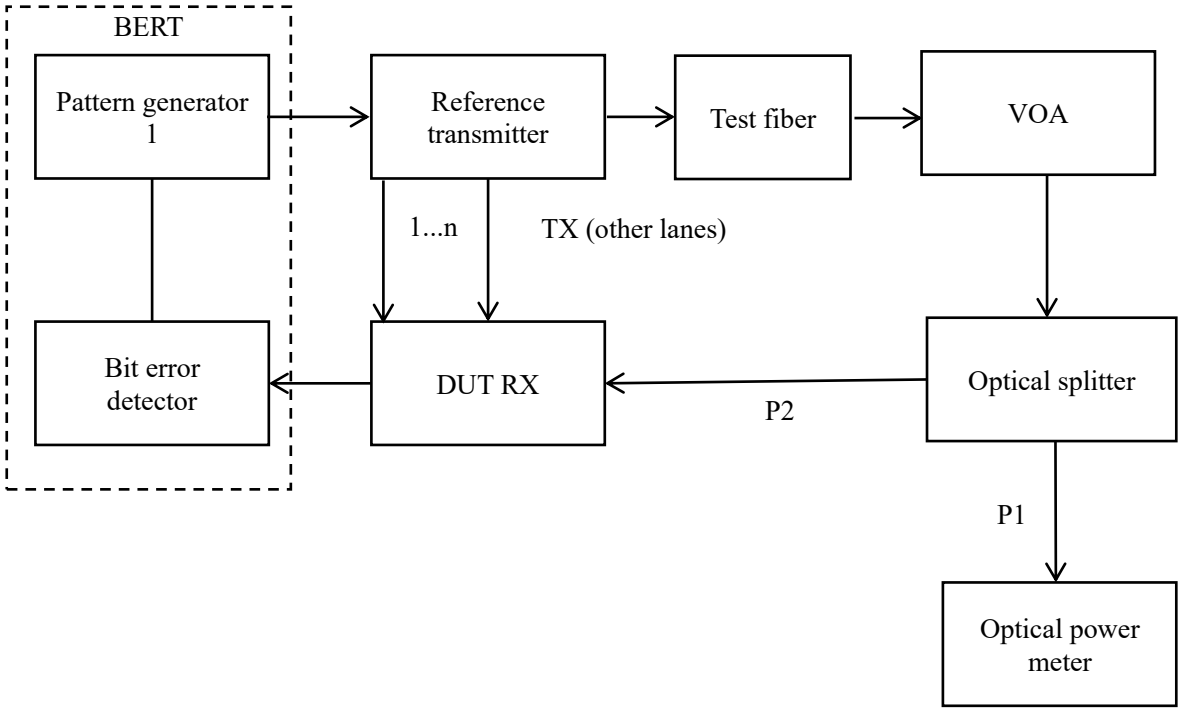


Figure 6-37 Receiver sensitivity with fiber propagation test

6.36.3 Test Steps

a Connect the test system according to Figure 6-37.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Measure the optical power values of the two output ports of the splitter to P1 and P2 defined in Figure 6-37, and determine the optical power compensation value using the following equation: $\Delta P = P2 – P1$. Then the receive optical power(P2) of the DUT can be calculated as $P2=P1+\Delta P$.

e Adjust the optical attenuator to 0 dB and wait for 12 seconds. After confirming the phase lock of the **BERT**, wait until the BER is stable. Then record the BER after 12 seconds.

f Adjust the attenuation value of the **VOA** until the measured BER is around BER 1E-6.

Note: The step of adjusting the attenuation value is advised to be set at 0.5dB.

g Adjust the attenuation value of the **VOA** until the measured BER rests stably 2.4E-4.

Note: The step of adjusting the attenuation value is advised to be set at 0.1dB.

h The above receive optical power and the corresponding BER are drawn as a BER curve, according to which the receive optical power corresponding to the target BER is obtained, namely, the **'receiver sensitivity with fiber propagation'.**

i When for a multi-lane optical module, repeat the test for other lanes.

Note:

1 Refer to the notes of the receiver sensitivity test defined in 6.35.

2 The 0.47 dB/km at 1264.5 nm attenuation for optical fiber cables is derived from *Appendix I of ITU-T G.695*.

3 The 0.5 dB/km attenuation is provided for the outside plant cable as defined in ANSI/TIA 568-C.3.

4 The SECQ of reference transmitter's optical eye is 0.9 dB (an ideal input signal without overshoot). The test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter and RIN.

5 Recommended values for parameters of single-mode fiber and multimode fiber are shown in Table 6-5.

Table 6-5 Recommended values for parameters of (a)single-mode fiber and (b)multimode fiber

(a) Single-mode fiber

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.47 or 0.5	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm

Description	Value	Unit
Dispersion slope (max) (S_0)	0.093	ps/nm^{2}km

(b) Multimode fiber

Description	OM3	OM4	OM5	Unit
Nominal core diameter	50			μm
Nominal fiber specification wavelength	850			nm
Effective modal bandwidth (min)	2000	4700		MHz.km
Cabled optical fiber attenuation (max)	3.5			dB/km

6.37 Interzone BER

6.37.1 Definition

The **'interzone BER'** is defined as the error bit ratio of any optical power point per lane in the whole range from the overload point to the sensitivity point or from the sensitivity point to the overload point.

6.37.2 Block Diagram

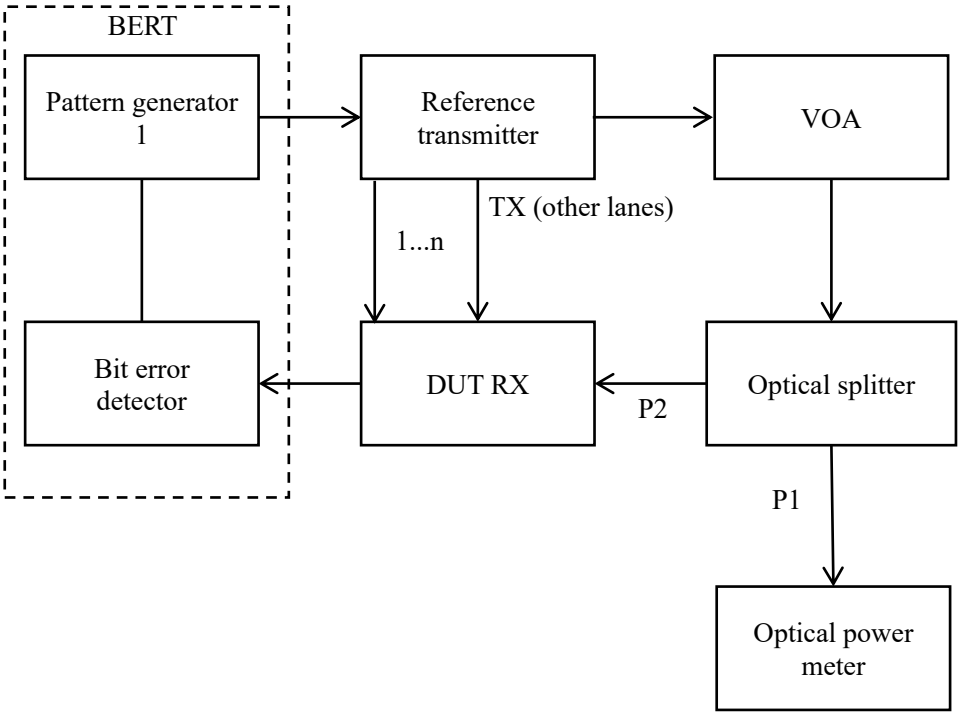


Figure 6-38 Interzone BER test

6.37.3 Test Steps

a Connect the test system according to Figure 6-38.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c Adjust the attenuation value of the **VOA** to the minimum value. Set the optical power values of the two output ports of the splitter to P1 and P2 defined in Figure 6-38, and determine the optical power compensation value using the following equation: ΔP = P2 – P1. Then the receive optical power(P2) of the **DUT** can be calculated as P2=P1+ΔP. Ensure that P2 is higher than the **'average receive power, each lane (max)'**.

d When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

e Adjust the attenuation value of the **VOA** to ensure that the receive optical power of DUT is at the sensitivity point.

f Adjust the attenuator value of the **VOA** to increase the receive optical power of the **DUT** until the receive power is near the DUT's overload point (specified '**overload receive optical power'** minus 1 dB).

Note: The step of adjusting the attenuator value is advised to be set at 0.5dB.

g Adjust the attenuator value of the **VOA** to increase the receive optical power of the **DUT** until the receive power is the **DUT**'s overload point. Read the BER at each point. Whenever the **VOA** adjustment is complete, wait a time interval until the BER at each point is stable and test the BER for 3 seconds at each point.

Note: The step of adjusting the attenuator value is advised to be set at 0.1dB.

h Draw the sensitivity curve of receive optical power and BER.

i When for a multi-lane optical module, repeat the test for other lanes.

Note:

1. Refer to the notes of the receiver sensitivity test defined in 6.35.
2. The SECQ of the reference transmitter's optical eye is 0.9 dB (an ideal input signal without overshoot). The test signal should have negligible impairments such as inter-symbol interference (ISI), rise/fall times, jitter and RIN.

6.38 LosA & LosD & Hysteresis

6.38.1 Definition

'The LosA' is defined as the maximum receive optical power per lane when the module enters the Rx LOS status. The unit is dBm.

'The LosD' is defined as the minimum receive optical power per lane when the module exits the Rx LOS status. The unit is dBm.

Hysteresis is **'LosD'** minus **'LosA'**. The unit is dB.

6.38.2 Block Diagram

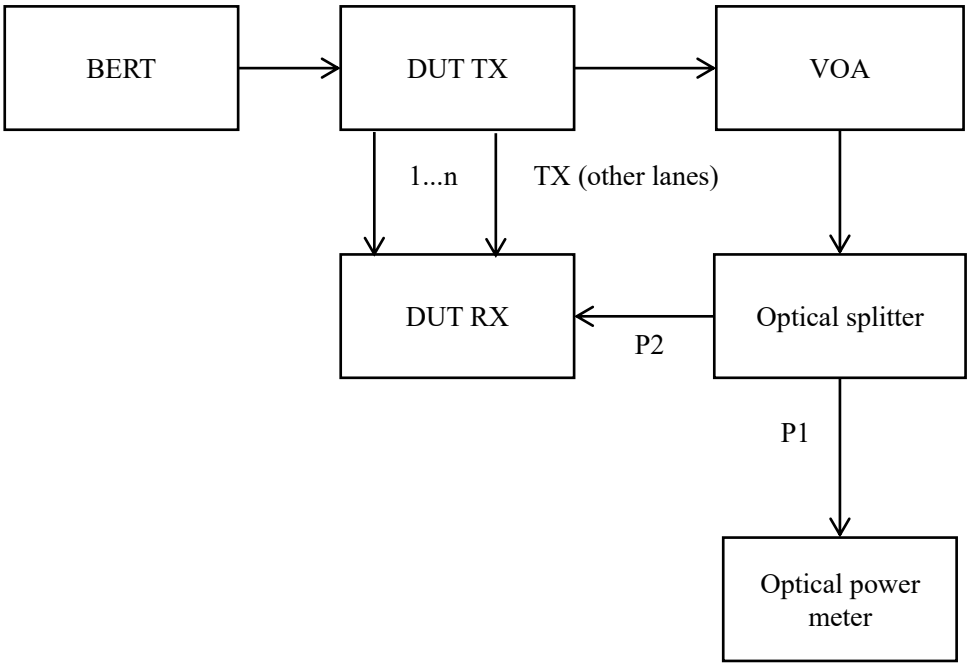


Figure 6-39 LosA & LosD & Hysteresis test

6.38.3 Test Steps

a Connect the test system according to Figure 6-39.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6-2.

c Adjust the attenuation value of the **VOA** to the minimum value. Set the optical power values of the two output ports of the **Optical splitter** to P1 and P2 defined in Figure 6-39, and determine the optical power compensation value using the following equation: $\Delta P = P2 - P1$.

d When for a multi-lane optical module, ensure that each optical lane is tested individually by turning on only one laser under test or by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

e Adjust the attenuation value of the **VOA** so that the **DUT** enters the RX LOS status.

Note: The step of the attenuation value is advised to be set at 0.5dB.

f Adjust the attenuation value of the **VOA** to increase the receive power until the DUT exits the RX LOS status. Read the optical power on the **Optical power meter**. The result is '**LosA**' (optical power meter's reading + ΔP).

Note: The step of the attenuation value is advised to be set at 0.1dB.

g Adjust the attenuation value of the **VOA** to increase the receive power until the DUT enters the RX LOS status. Read the optical power on the **Optical power meter**. The result is '**LosD**' (optical power meter's reading + ΔP).

Note: The step of the attenuation value is advised to be set at 0.1dB.

h Calculate **'hysteresis'** is LosD minus LosA.

i When for a multi-lane optical module, repeat the test for other lanes.

7 Electrical Interfaces

The clause is organized into several methods for the industry to reference in electrical interface testing.

The 28G-NRZ and 112G-PAM4 test methods are not included in this clause. The 28G-NRZ test method is mature and the 112G-PAM4 test method has only a draft version. This standard only reflects the test specifications of 56G-PAM4.

7.1 Module Output

7.1.1 Test Item

The test items of this clause are shown in Table 7-1.

Table 7-1 Module-to-host electrical test parameters at TP4 (module output)

Parameter	Unit
Differential voltage, pk-pk	mV
Common mode noise, RMS	mV
Differential termination resistance mismatch	%
Transition time	ps
Near-end eye width at 10^{-6} probability (EW6)	UI
Near-end eye height at 10^{-6} probability (EH6)	mV
Far-end eye width at 10^{-6} probability (EW6)	UI
Far-end eye height at 10^{-6} probability (EH6)	mV
Near-end eye linearity	-

7.1.2 Crosstalk Signal Calibration

a Connect the test system according to Figure 7-1.

b Use a QPRBS13-CEI pattern to calibrate the crosstalk signal at TP1a.

c The amplitude and slew time of the crosstalk source are listed in Table 7-2.

Table 7-2 Crosstalk parameters for module output test calibration at TP1a

Parameter	Target Value	Unit
Crosstalk amplitude differential voltage pk-pk	900	mV
Crosstalk slew time (between –270 mV and +270 mV)	19	ps

7.1.3 Block Diagram

The output eye width and eye height of the module are tested at TP4 using a module compliance board. Figure 7-1 shows the test setup.

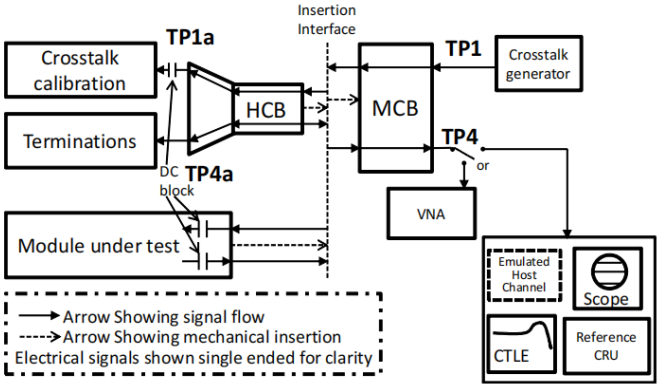


Figure 7-1 Module output test setup

7.1.4 Test Steps

Connect the test system according to Figure 7-1. Add the pattern generator at TP1 and use the data pattern QPRBS13-CEI. Add crosstalk generators at all other lanes. Connect TP2 and TP3 of the optical module with a short optical fiber. The tested signal at TP4 is transmitted to the oscilloscope and the reference CRU with a microwave pike-off. The CRU uses a first-order transfer function with a 3 dB tracking bandwidth of fb/6640. Configure the oscilloscope to collect 10 samples/UI and 2048 samples/waveform. Stop the test when 10 patterns and 100 waveforms are collected.

7.1.4.1 Output Differential Voltage, pk-pk

a The waveform is observed through a fourth-order Bessel-Thomson filter response with a bandwidth of 40 GHz.

b Set the oscilloscope to operate in eye/mask mode. Set up a vertical histogram with full display width.

c The value of **'output differential voltage, pk-pk'** is the pk-pk value of the histogram.

d For a 400G optical module, repeat the test for other lanes.

7.1.4.2 Common Mode Noise

a The oscilloscope bandwidth shall be 40 GHz.

b Waveforms are not triggered (free-run mode). The oscilloscope shall have a minimum bandwidth (including probes) of 1.8 times the signaling rate.

c The sum of the two inputs is obtained for common mode analysis. Set the horizontal scale for full width to span one UI. Set up a vertical histogram with full display width.

d Measure the RMS value of the histogram. **'Common mode Noise'** value is half the RMS value of the histogram.

e For a 400G optical module, repeat the test for other lanes.

7.1.4.3 Transition Time

a The waveform is observed through a fourth-order Bessel-Thomson filter response with a bandwidth of 40 GHz.

b ‘**Transition times’** (rise and fall times) are defined as the time between the 20% and 80% times, or 80% and 20% times, respectively, of isolated –1 to +1 or +1 to –1 PAM4 edges.

c The transitions within sequences of three –1s followed by three +1s, and three +1s followed by three –1s, respectively, are measured.

d For a 400G optical module, repeat the test for other lanes.

7.1.4.4 Eye Width, Eye Height and Eye Linearity

a The waveform is observed through a fourth-order Bessel-Thomson filter response with a bandwidth of 40 GHz.

b Capture the differential signal at TP4 with an oscilloscope triggered with a clock from a reference CRU by applying a first-order transfer function and a 3 dB tracking bandwidth of fb/6640.

c Set the oscilloscope to operate in jitter/noise mode. Set the measurement probability to 10-6.

d A reference receiver with a CTLE is used to measure the eye width and eye height. Add a linearity test.

e For the near-end compliance test, the CTLE peaking in the reference receiver shall be set at 1dB, 1.5dB, or 2dB. Any CTLE setting that meets both the EH6 and EW6 settings defined for TP4 in Table 6-1 is acceptable.

f For the far-end compliance test, the signal measured at TP4 is first convolved with an emulated loss lane (around 7 dB loss at fb/2) that represents the worst-case lane loss. The CTLE peaking in the reference receiver shall be set from 1dB to 9dB. Any CTLE setting that meets both the EH6 and EW6 requirements defined for far-end TP4 in Table 6-1 is acceptable.

g Measure the ‘eye width’, ‘eye height’ and ‘eye linearity’ on the oscilloscope.

h For a 400G optical module, repeat the test for other lanes.

7.2 Module Stressed Input

The ability of the module input to tolerate the eye width, eye height, and eye linearity specified in Table 7-5 and the sinusoidal jitter specified in Table 7-6 is tested.

7.2.1 Module Input Signal Calibration

a Connect the test system according to Figure 7-2.

b Generate a loss of 12.2 dB at Nyquist to TP1a from the output of a pattern generator with a nominal rise/fall time of 10.5 ps.

c Use a QPRBS13-CEI pattern to calibrate the stressed input test signal at TP1a and the crosstalk signal at TP4.

d The amplitude and slew time of the crosstalk source are listed in Table 7-3.

e Sinusoidal jitter (10x the reference CRU's bandwidth) and UUGJ are added to a clean test pattern until the jitter (except for EOJ) at the output of the pattern generator approximates the informative transmit recommendations listed in Table 7-4.

f The optimal CTLE peaking value is defined as the setting that results in the maximum value of EW6*EH6. Adjust the pattern generator output to make this optimal CTLE peaking value higher than or equal to 7dB.

g Adjust the UUGJ and pattern generator amplitude to generate the minimum eye height and eye width and minimum eye linearity specified in Table 7-5. (The upper and lower PAM4 eyes are adjusted to be smaller than the middle eye and configured to meet the minimum eye height and eye width requirement.)

Table 7-3 Crosstalk parameters for module stressed input test calibration at TP4

Parameter	**Target Value**	**Unit**
Crosstalk amplitude differential voltage, pk-pk	900	mV
Crosstalk slew time (between –270 mV and +270 mV)	9.5	ps

Table 7-4 Host-to-module electrical recommendations at TP0a

Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
Differential voltage, pk-pk	T_Vdiff	750	-	mV
Transition time: 20% to 80%	T_tr, T_tf	7.5	-	ps
Common mode noise, RMS	T_Ncm	-	12	mV
Uncorrelated Unbounded Gaussian Jitter (UUGJ)			0.01	UI_{RMS}
Uncorrelated Bounded High Probability Jitter (UBHPJ)			0.05	UI
Even-Odd Jitter (EOJ)			0.019	UI
Signal-to-noise-and-distortion ratio		31	-	dB

Table 7-5 Host-to-module electrical specifications at TP1a (host output)

Parameter	**Min.**	**Max.**	**Unit**
Eye width at 10^{-6} probability (EW6)	0.20	-	UI
Eye height at 10^{-6} probability (EH6)	32	-	mV
Eye linearity	0.85	-	-

7.2.2 Block Diagram

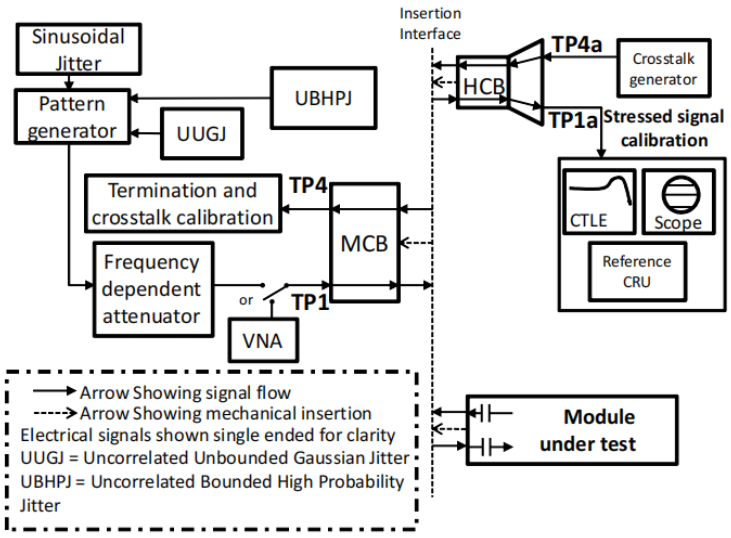


Figure 7-2 Module input test setup

7.2.3 Test Steps

a Connect the test system according to Figure 7-2.

b Connect TP2 and TP3 of the optical module with a short optical fiber.

c Add the pattern generator at TP1 and use the data pattern QPRBS31-CEI.

d Add crosstalk generators at all other lanes.

e Set the sinusoidal jitter to fCRU/100, fCRU/3, fCRU, 3fCRU, and 10fCRU. fCRU is the jitter corner frequency given by fb/6640.

f The module shall achieve a raw BER of 10-6 or better in the stressed input test at TP4.

g For a 400G optical module, repeat the test for other lanes.

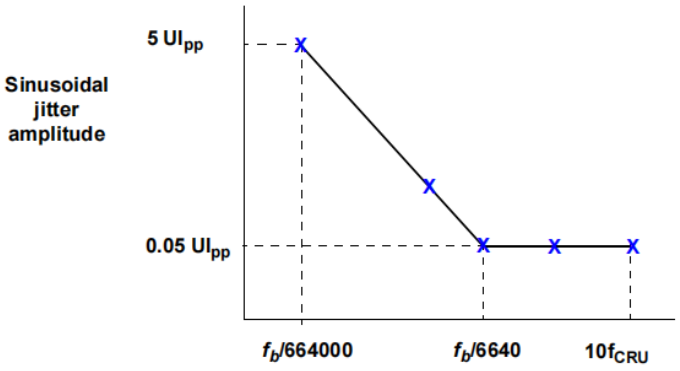


Figure 7-3 Module input sinusoidal jitter

Table 7-6 Sinusoidal jitter frequency for TP1a testing

Frequency Range	Sinusoidal Jitter, Peak-to-Peak (UI)
f < f_b/664000	Not specified
f_b/664000 < f ≤ f_b/6640	5·f_b/(664000·f)
f_b/6640 < f ≤ 10f_{CRU}	0.05

7.3 Mated HCB and MCB S-parameters

The reference mated MCB-HCB loss is given in Equation 7-1.

Equation 7-1: $SDD21, SDD12 = (-0.475)\sqrt{f} - 0.1204 f - 0.002 f^2$

(0.05 GHz < f < 29.0 GHz, f is frequency in GHz, loss in dB)

The FOMILD for the mated HCB and MCB pair is ≤ 0.1 dB.

8 Power Consumption

The clause is organized into the method for the industry to reference in power consumption testing.

8.1 Definition

Power consumption is defined as the product of normal working voltage and current of a transceiver, and the unit is W.

Note:

Module power consumption generally refers to the maximum consumption value of the module operating in the full temperature range (for example, the operating temperature range of an industrial module is from –40°C to +85°C, and that of a commercial module is from 0°C to 70°C) and voltage range (for example, from 3.13 V to 3.47 V).

8.2 Block Diagram

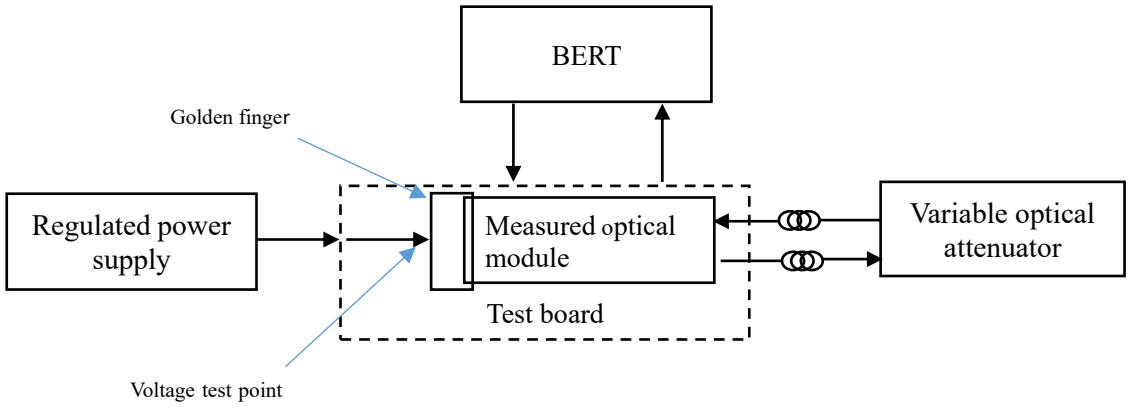


Figure 8-1 Power consumption test

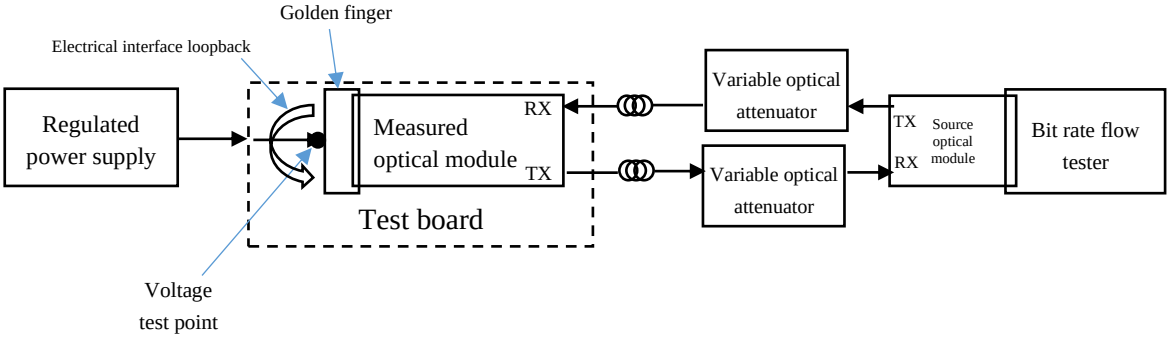


Figure 8-2 Power consumption test

8.3 Test Steps

a Connect the test system according to Figure 8-1 or Figure 8-2.

b Set the rate, pattern, and amplitude for the output modulation signals of the BERT or bit rate flow tester. The setup is defined in Table 8-1 and Table 8-2.

Table 8-1 BERT setup

Category	Test Pattern	Lane	Data Rate (electrical interfaces)	Modulation Format	Note
100G DR1 QSFP28	PRBS31	4	26.5625 Gbit/s	NRZ	2
100G FR1 QSFP28	PRBS31	4	26.5625 Gbit/s	NRZ	2
100G LR1 QSFP28	PRBS31	4	26.5625 Gbit/s	NRZ	2
100G ER1 QSFP28	PRBS31	4	26.5625 Gbit/s	NRZ	2
400G DR4 QSFP-DD	PRBS31Q	8	53.125 Gbit/s	PAM4	2
400G FR4 QSFP-DD	PRBS31Q	8	53.125 Gbit/s	PAM4	2
400G LR4 QSFP-DD	PRBS31Q	8	53.125 Gbit/s	PAM4	2
400G DR4 QSFP112	PRBS31Q	4	106.25 Gbit/s	PAM4	2
400G FR4 QSFP112	PRBS31Q	4	106.25 Gbit/s	PAM4	2
400G LR4 QSFP112	PRBS31Q	4	106.25 Gbit/s	PAM4	2

Table 8-2 Bit Rate Flow Tester Setup

Category	Test Pattern	Lane	Data Rate	Modulation Format	Note
100G DR1 QSFP28	100GE	4	25.78125 Gbit/s	NRZ	1
100G FR1 QSFP28	100GE	4	25.78125 Gbit/s	NRZ	1
100G LR1 QSFP28	100GE	4	25.78125 Gbit/s	NRZ	1
100G ER1 QSFP28	100GE	4	25.78125 Gbit/s	NRZ	1

Category	Test Pattern	Lane	Data Rate	Modulation Format	Note
100G DR1 QSFP28	100GE	4	26.5625 Gbit/s	NRZ	2
100G FR1 QSFP28	100GE	4	26.5625 Gbit/s	NRZ	2
100G LR1 QSFP28	100GE	4	26.5625 Gbit/s	NRZ	2
100G ER1 QSFP28	100GE	4	26.5625 Gbit/s	NRZ	2
400G DR4 QSFP-DD	400GE	8	53.125 Gbit/s	PAM4	2
400G FR4 QSFP-DD	400GE	8	53.125 Gbit/s	PAM4	2
400G LR4 QSFP-DD	400GE	8	53.125 Gbit/s	PAM4	2
400G DR4 QSFP112	400GE	4	106.25 Gbit/s	PAM4	2
400G FR4 QSFP112	400GE	4	106.25 Gbit/s	PAM4	2
400G LR4 QSFP112	400GE	4	106.25 Gbit/s	PAM4	2

c Set the regulated power supply and output the specified voltage and current within the ranges.

d Adjust the variable optical attenuator so that the optical power entering the measured optical module receiver is within the normal operating range, to ensure that the measured optical module works properly.

e Use a multimeter to test the voltage at the voltage test point as close as possible to the golden finger and read the current values of the regulated power supply and multiply them to obtain the power consumption.

Note:

1. FEC function is enabled on the module under test. For details, see Figure 8-2.
2. FEC function is not enabled on the module under test. For details, see Figure 8-1 or Figure 8-2.

9 Management Interfaces

The clause is organized into several methods for the industry to reference in management interface testing.

9.1 Definition

The I2C-Based Management Communication Interface (I2CMCI) is implemented as the management interface which allows the host to manage the module's functionality and operation. I2CMCI consists of a clock signal (SCL), a data signal (SDA), and a module selection signal (MODSel).

9.2 Test Block Diagram

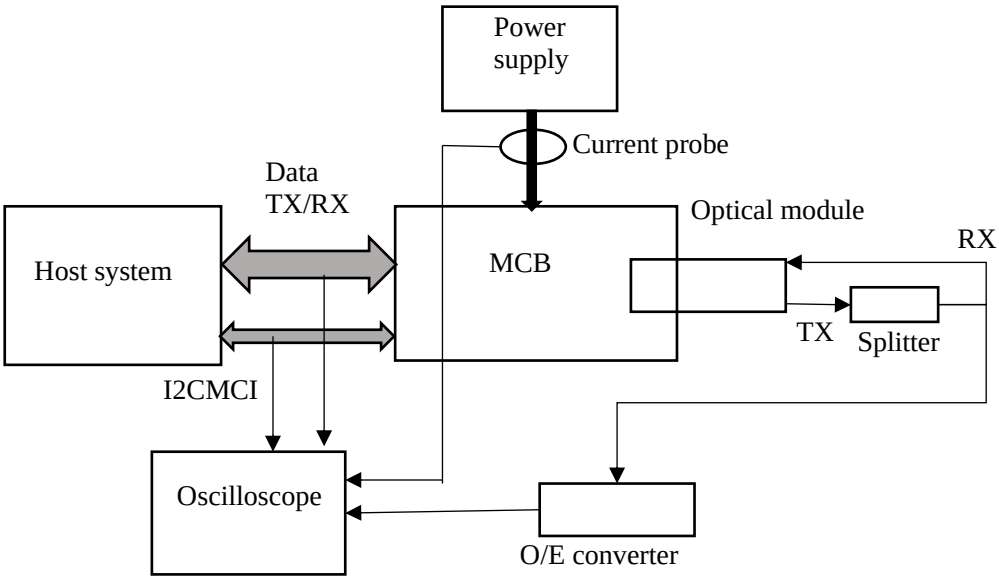


Figure 9-1 Management interface test

9.2.1 I2CMCI Read/Write/Test

The host system asserts MODSel and uses the following operations to access the optical module through I2CMCI at a 0–400 kHz (1 MHz if supported) SCL clock speed. The clock stretch duration is 500 µs, and the results should be obtained successfully. In addition to 100K and 400K, other typical speeds such as 20K, 50K, and 200K should be used to confirm I2CMCI robustness.

a Read one byte from the current byte address.

b Read n > 1 bytes sequentially, starting at the current byte address.

c Read one byte from a given byte address.

d Read n > 1 bytes sequentially, starting at a given byte address.

e Write one byte to a given address.

f Write n > 1 bytes sequentially, starting at a given byte address.

g Test if target is ready to accept transaction (ACK polling).

Note:

1. The optical module maintains the internal address counter to roll-over in lower memory and sets the current byte address to 0 when the address to be incremented is 127. To roll-over in upper memory, the optical module sets the current byte address to 128 when the address to be incremented is 255.
2. These tests should be performed in both low-power mode and high-power mode.

9.3 I2CMCI Transaction Timing

Once the host system starts a new I2CMCI transaction 80ms after writing up to 8 bytes to a non-volatile memory or register, it should get a successful result.

Once the host system starts a new I2CMCI transaction 10ms after writing to a volatile memory or register, it should get a successful result.

Once the host system starts a new I2CMCI transaction 10ms after writing to Page Mapping register (Bank Select/Page Select), it should get a successful result.

Once the host system starts a new I2CMCI transaction 20 μs after a Read operation, it should get a successful result.

Note: For a QSFP28 module, if it cannot pass the preceding tests, its specific specification in the following sections should be met.

9.4 MODSel

Once the host system de-asserts MODSel and starts a I2CMCI transaction, it should not get any response from the optical module.

Once the host system asserts MODSel (ModSelL setup time >2ms, ModSelL hold time < 500μs) 2ms after MODSel de-asserting and does any I2CMCI transaction, it should get a successful result.

9.5 QSFP28 Module Related Test

For a QSFP28 module, the following timing and register test (defined in 9.5.1,9.5.2,9.5.3) should be performed and the timing must meet the specification. The settings and functions of the register should be correct.

9.5.1 Timing

Table 9-1 Test parameters and test criteria of timing

Parameter	Symbol	Unit	Test Criteria
Initialization Time	t_init	s	Time from power on or hot plug until the module is fully functional (hereafter defined as Tx output OMA rises to 90% of nominal) and Rx CDR Loss of Lock (LOL) flag is deasserted (to the STOP condition of the I2C read of Rx LOL). This time applies to Power Class 2 or higher modules when LPMode is pulled low by the host, and to all Power Class 1 modules.
Reset Init Assert Time	t_reset_init	μs	The host is required to provide a reset pulse of at least the minimum value for the module to guarantee a reset sequence. The module should be reset by the minimum reset pulse successfully. Shorter pulses may reset the module depending on implementation.
Serial Bus Hardware Ready Time	t_serial	s	Time from power on until the module responds to data transmission over the two-wire serial bus, measured by the start condition for the first acknowledged I2C transaction.
Reset Assert Time	t_reset	s	Time from a rising edge on the ResetL input until the module is fully functional.
LPMode/TxDis mode change time	t_LPMode/TxDis	ms	Time to change between LPMode and TxDis modes of the dual-mode signal LPMode/TxDis. It can be tested by putting the module in high power state with LPMode/TxDis set to High (use power override). The TX output ON/OFF is measured by switching LPMode and TxDis. Tx ON/OFF

Parameter	Symbol	Unit	Test Criteria
			operation time can be subtracted here because only mode change time is counted here.
LPMode Assert Time	ton_LPMode	ms	Time from when the host releases LPMode to high until module power consumption reaches Power Class 1, hereafter defined as current less than 455 mA (3.3 V).
LPMode Deassert Time	toff_LPMode	ms	Time from when the host pulls LPMode low until the module is fully functional.
IntL Assert Time	ton_IntL	ms	Time from occurrence of condition triggering an interruption (such as Rx low Alarm/Waring, Rx LOL) until IntL is low.
IntL Deassert Time	toff_IntL	µs	Time from clear on read operation (measured from the STOP condition of I2C read) of associated flag until the module releases IntL to high. This includes the time to clear Rx LOS, Tx Fault, and other flag bits.
IntL/RxLOSL mode change time	t_IntL/RxLOSL	ms	Time to change between IntL and RxLOSL modes of the dual-mode signal IntL/RxLOSL. It can be tested by switching between IntL and RxLOSL after setting up all interrupts mask bits when Rx LOS is happening. The time is measured from the STOP condition of I2C write to the rising/falling edge of IntL/RxLOSL.
RxLOSL Assert Time (Optional Fast Mode)	ton_f_LOS	ms	Optional fast mode is advertised via the management interface (SFF-8636). It is the time from when the optical loss of signal (hereafter defined as Rx input signal) falls below the loss threshold until RxLOSL signal is pulled low by the module.
Rx LOS Assert Time	ton_LOS	ms	Time from Rx optical signal loss to Rx LOS bit set to 1 and IntL pulled low by the module.
RxLOSL Deassert Time (Optional Fast Mode)	toff_f_LOS	ms	Optional fast mode is advertised via the management interface (SFF-8636). It is the time from when the optical signal is above the LOS deassert threshold until the module releases the RxLOSL signal to high.
Power_override or Power_set Assert Time	ton_Pdown	ms	Time from Power_override or Power_Set bit set to 1 (measured from the STOP condition of the I2C write) until module power consumption reaches Power Class 1.
Power_override or Power_set Deassert Time	toff_Pdown	ms	Time from Power_override or Power_Set bit cleared to 0 (measured from the STOP condition of the I2C write) until the module is fully functional.
Rx Squelch Assert Time	ton_Rxsq	ms	Time from loss of Rx input signals until the squelched output condition is less than 50 mVpp.
Rx Squelch Deassert Time	toff_Rxsq	ms	Time from resumption of Rx input signals until normal Rx output condition is reached.
Tx Squelch Assert Time	ton_Txsq	ms	Time from loss of Tx input signal (less than 50 mVpp) until the squelched output condition (application dependent, OMA less than or equal to –26 dBm or average power less than or equal to –30 dBm) is reached.

Parameter	Symbol	Unit	Test Criteria
Tx Squelch Deassert Time	toff_Txsq	ms	Time from resumption of Tx input signals until normal Tx output condition is reached.
Tx Disable Assert Time	ton_TxDis	ms	Time from Tx Disable bit set to 1 (measured from the STOP condition of the I2C write) until optical output falls below 10% of nominal.
Tx Disable Deassert Time	toff_TxDis	ms	Time from Tx Disable bit cleared to 0 (measured from the STOP condition of the I2C write) until optical output rises to above 90% of nominal.
Rx Output Disable Assert Time	ton_RxDis	ms	Time from Rx Output Disable bit set to 1 (measured from the STOP condition of the I2C write) until Rx output falls below 10% of nominal.
Rx Output Disable Deassert Time	toff_RxDis	ms	Time from Rx Output Disable bit cleared to 0 (measured from the STOP condition of the I2C write) until Rx output rises to above 90% of nominal.
ModSelL Setup Time (Note 1)	Host_select_setup	ms	Setup time on the select lines before a host initiates the serial bus sequence.
ModSelL Hold Time (Note 1)	Host_select_hold	µs	Delay from completion of a serial bus sequence to ModSelL rising edge.
Aborted sequence – bus release	Deselect_Abort	ms	Delay from a host setting ModSelL to high (at any point in a bus sequence) to the QSFP module releasing SCL and SDA.
Complete Single or Sequential Write	tWR	ms	Complete a sequential write of up to four bytes. It can be tested by a continuous writing with 40 ms delay and all the data should be written successfully.

9.5.2 Management Interface Timing

Table 9-2 Test parameter and test criteria of management interface timing

Parameter	Symbol	Unit	Test Criteria
Clock Frequency	fSCL	kHz	TBD
Clock Pulse Width Low	tLOW	µs	TBD
Clock Pulse Width High	tHIGH	µs	TBD
Time bus free before new transmission can start	tBUF	µs	Between STOP and START and between ACK and Restart
START Hold Time	tHD.STA	µs	TBD
START Set-up Time	tSU.STA	µs	TBD
Data in Hold Time	tHD.DAT	µs	TBD

Parameter	Symbol	Unit	Test Criteria
Data in Set-up Time	tSU.DAT	µs	TBD
Input Rise Time (400 kHz)	tR.400	ns	From (VIL, MAX – 0.15) to (VIH, MIN + 0.15)
Input Fall Time (400 kHz)	tF.400	ns	From (VIH, MIN + 0.15) to (VIL, MAX – 0.15)
STOP Set-up Time	tSU.STO	µs	TBD
Clock Holdoff Time (Clock Stretching)	T_clock_hold	µs	Maximum time the module may hold SCL low before completing a read or write operation

9.5.3 Register Test

This clause reference *SFF-8636 Rev2.10a*.

Table 9-3 Lower Page 00H

Byte	Name	Description
86	Tx4-1_Rate_select	Disable Read/Write bit for software disable of Tx4-1.
87	Rx4-Rx1_Rate_select	Software rate select. Rx Channel 4-1 MSB&LSB.
88	Tx4-1_Rate_select	Software rate select. Tx Channel 4-1 MSB&LSB.
93	SW Reset & Power Control	Software reset, High Power Class Enable, Power set and Power override.
d98	TX&RX CDR Control	Channel 4-1 TX&RX CDR control.
99	LP/Dis, IntL/LOSL ctrl	LPMode/TxDis input signal control. IntL/LOSL output signal control.
115	ModSelL wait time	The ModSelL wait time is the mantissa x 2^exponent expressed in microseconds.

Table 9-4 Upper Page 00H

Byte	Name	Description
193	Option Functions Ad.	The advertisement of the implement of LPMode/TxDis, IntL/RxLOSL output, Tx input adaptive equalizers freeze capable, Tx input equalizers auto-adaptive capable, Tx input equalizers fixed-programmable settings. Rx output emphasis fixed-programmable settings, Rx output amplitude fixed-programmable settings.
194	Option Functions Ad.	The advertisement of the implement of Tx CDR On/Off Control, Rx CDR On/Off Control, Tx CDR Loss of Lock (LOL) flag, Rx CDR Loss of Lock (LOL) flag, Rx Squelch Disable, Rx Output Disable, Tx Squelch Disable, Tx Squelch.
195	Option Functions Ad.	The advertisement of the implement of Memory Page 01/02, Rate select, Tx_Disable, Tx_Fault, Tx Squelch, Tx Loss, Pages 20-21h.
221	Advanced Function Ad.	The advertisement of the implement of Initialization Complete Flag, Rate Selection, TC readiness flag, Software reset.

Table 9-5 Page 03H

Byte	Name	Description
224-225	EQ, emphasis, amplitude Ad.	The advertisement of the implement of Max Tx input equalization, Max Rx output emphasis, Rx output emphasis type, Rx output amplitude.
227	FEC, TX Sqelch, RxLOSL, TxDis Ad.	The advertisement of the implement of the capability to terminate and generate FEC encoding from and to the host/media, Tx Force Squelch, RxLOSL Fast Mode, TxDis Fast Mode.
230	FEC Control	Enable/Disable host-side FEC termination on the Tx electrical inputs and host-side FEC generation on the Rx electrical outputs, enable/disable media-side FEC generation on the Tx outputs and media-side FEC termination on the Rx inputs.
231	Tx Force Squelch Control	Software squelch of transmitter output, per media lane
234-235	Tx Input Equalizer Control	Tx input equalizer controls
236-247	Rx output emphasis controls	Rx1-4 output emphasis controls
238-239	Rx output amplitude control	Controls for Rx1-4 output differential amplitude
240	Rx/TX SQ Control	Controls to disable squelch of Rx1-4/Tx1-4 outputs
241	Rx Output, Tx adaptive equalization Control	Controls to disable Rx1-4 outputs, Tx1-4 input adaptive equalizers

9.6 QSFP-DD Module Related Tests

For QSFP-DD module, the following timing and register test (defined in 9.6.1,9.6.2,9.6.3) should be implemented. The timing must meet the specification and the register corresponding settings and functions should be correct.

For CDB part, the following Command ID should be test.

9.6.1 Timing

This clause reference *QSFP-DD Hardware Specification Rev5.1*.

Table 9-6 Test parameters and test criteria of timing

Parameter	Symbol	Unit	Test Criteria
MgmtInitDuration	Max MgmtInit Duration	ms	Time from power on, hot plug, or rising edge of reset to the high-to-low SDA transition as the start condition for the first acknowledged TWI transaction.
ResetL Assert Time	t_reset_init	µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL	ms	Time from occurrence of condition, such as Rx LOS, Rx LOL, triggering IntL until Vout:IntL =

Parameter	Symbol	Unit	Test Criteria
			Vol.
IntL Deassert Time	toff_IntL	µs	Time from clear on read operation of associated flag (measured from the STOP condition of the I2C read) until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault, and other flag bits.
Rx LOS Assert Time	ton_los	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted
Module Select Wait Time	ModSelWaitTime	-	ModSel wait time as m·2e in µs 00h: no data available
Data Path Init Max Duration	DataPathInit_MaxDuration	-	Maximum duration of the DPInit state; i.e., data path from Deactivated to Initialized mode, measured from the STOP condition of I2C write of DP initialization control to the STOP condition of I2C read of DP States.
Data Path Deinit Max Duration	DataPathDeinit_MaxDuration	-	Maximum duration of the DPDeinit state; i.e., data path from Initialized to Deactivated mode, measured from the STOP condition of I2C write of DP initialization control to the STOP condition of I2C read of DP States.
Module Pwr Up Max Duration	ModulePwrUp_MaxDuration	-	Encoded maximum duration of the ModulePwrUp state; i.e., module from low power mode state to ModuleReady state, measured from the STOP condition of I2C write of LowPwrRequestSW to the STOP condition of I2C read of ModuleState.
Module Pwr Dn Max Duration	ModulePwrDn_MaxDuration	-	Encoded maximum duration of the ModulePwrDn state; i.e., module from ModuleReady state to low power mode state, measured from the STOP condition of I2C write of LowPwrRequestSW to the STOP condition of I2C read of ModuleState.
Rx Squelch Assert Time	ton_Rxsq	ms	Time from loss of Rx input signal until the squelched output is less than 50 mVpp.
Tx Squelch Assert Time	ton_Txsq	ms	Time from loss of Tx input signal (less than 70 mVpp) until the squelched output condition (application dependent: average power or OMA) is reached.

Parameter	Symbol	Unit	Test Criteria
Tx Squelch Deassert Time	toff_Txsq	s	Time from Tx input signal rises to above 90% of nominal until optical output rises to above 90% of nominal.
Tx Disable Assert Time	ton_txdis	ms	Time from the STOP condition of the Tx Disable write sequence1 until optical output falls below 10% of nominal.
Tx Disable Assert Time (optional fast mode)	ton_txdisf	ms	Time from Tx Disable bit set (value = 1b, measured from the STOP condition of I2C write) until optical output falls below 10% of nominal.
Tx Disable Deassert Time	toff_txdis	ms	Time from Tx Disable bit cleared (value = 0b, measured from the STOP condition of I2C write) until optical output rises to above 90% of nominal.
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	ms	Time from Tx Disable bit cleared (value = 0b, measured from the STOP condition of I2C write) until optical output rises to above 90% of nominal.
Rx Output Disable Assert Time	ton_rxdis	ms	Time from Rx Output Disable bit set (value = 1b, measured from the STOP condition of I2C write) until Rx output falls below 10% of nominal.
Rx Output Disable Deassert Time	toff_rxdis	ms	Time from Rx Output Disable bit cleared (value = 0b, measured from the STOP condition of I2C write) until Rx output rises to above 90% of nominal.

9.6.2 Management Interface Timing

Table 9-7 Test parameters and test criteria of management interface timing

TWI Modes			
Parameter	**Symbol**	**Unit**	**Test Criteria**
Clock Frequency	fSCL	kHz	NA
Clock Pulse Width Low	tLOW	μs	NA
Clock Pulse Width High	tHIGH	μs	NA
Time bus free before new transmission can start	tBUF	μs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	μs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	μs	The delay required between SCL becoming high and SDA starting to go low in a START

TWI Modes			
Parameter	**Symbol**	**Unit**	**Test Criteria**
Data In Hold Time	tHD.DAT	µs	NA
Data In Setup Time	tSU.DAT	µs	NA
Input Rise Time	tR	ns	From (VL,MAX = 0.3*Vcc) to (VIH,MIN = 0.7*Vcc)
Input Fall Time	tF	ns	From (VIH,MIN = 0.7*Vcc) to (VIL,MAX = 0.3*Vcc)
STOP Setup Time	tSU.STO	µs	NA
STOP Hold Time	tHD.STO	µs	NA
Aborted sequence – bus release	Deselect _Abort	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time	tSU.ModSelL	ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated serial bus sequence.
ModSelL Hold Time	tHD.ModSelL	ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module select status.
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold	µs	Time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to non-volatile registers	tWR	ms	Time to complete a Single or Sequential Write to non-volatile registers.
Accept a single or sequential write to volatile memory	tNACK	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC	ms	Time to complete a memory bank and/or page change.

Note: Endurance (write cycles) is ignored here.

9.6.3 Register Test

This clause reference *CMI Rev5.0*.

Table 9-8 Lower Memory

Byte	Summary	Description
2	MemoryModel, SteppedConfigOnly, MciMaxSpeed	Indicator of the memory model of the module, intervention-free or step-by-step reconfiguration, maximum supported clock speed of Management Communication Interface (MCI)
26	LowPwrAllowRequestHW, SquelchMethodSelect, LowPwrRequestSW,	Enable/Disable the evaluation of the LowPwrRequestHW hardware signal,

Byte	Summary	Description
	SoftwareReset	Squelching of Tx output reduces OMA/Pav, Request for the module to stay in, or to return into, Low Power mode, SoftwareReset triggers the module to be reset.
86-117	AppDescriptors	AppDescriptor AppSel 1-8

Table 9-9 Page 01H

Byte	Summary	Description
143	ModSelWaitTime	ModSel wait time as m·2e in µs
144	MaxDurationDPDeinit/DPInit	Maximum duration of the DPDeinit/DPInit state
151	OpticalDetectorType, RxOutputEqType, RxPowerMeasurementType, RxLOSType, RxLOSIsFast, TxDisableIsFast, TxDisableIsModuleWide	OpticalDetectorType of PIN/APD, RxOutputEqType of Peak-to-peak (p-p) amplitude stays constant, Steady-state amplitude stays constant, Average of p-p and steady-state amplitude stays constant, RxPowerMeasurementType of OMA/average power, Rx LOS responds to OMA/Pav, Module raises Rx LOS within "fast mode" timing limits, Module responds to Tx Output Disable in "fast mode" timing limits, Tx output disable is controlled per lane/all lanes together.
153	RxOutputLevelSupported, TxInputEqMax	RxOutputLevel Amplitude Code 0-3 not supported/supported, Maximum supported value of the Tx Input Equalization control for manual/fixed programming
154	RxOutputEqPostCursorMax, RxOutputEqPreCursorMax	Maximum supported value of the Rx Output Eq Post-cursor/Pre-cursor control

Byte	Summary	Description
155	WavelengthIsControllable, TransmitterIsTunable, SquelchMethodTx, ForcedSquelchTxSupported, AutoSquelchDisableTxSupported, OutputDisableTxSupported, InputPolarityFlipTxSupported	Active wavelength control supported, Transmitter is tunable, Tx output squelching function reduces OMA/Pav, Host cannot/can force squelching of Tx outputs using OutputSquelchForceTx, Host cannot/can disable automatic squelching of Tx outputs using AutoSquelchDisableTx, Host cannot/can disable Tx outputs using the OutputDisableTx register, InputPolarityFlipTx control not supported/supported
156	AutoSquelchDisableRxSupported, OutputDisableRxSupported, OutputPolarityFlipRxSupported	Host cannot/can disable automatic squelching of Rx outputs using AutoSquelchDisableRx, Host cannot/can disable Rx outputs using the OutputDisableRx register, PolarityFlipRx not supported/supported.
157	AdaptiveInputEqFailFlagTxSupported, CDRLOLFlagTxSupported, LOSFlagTxSupported, FailureFlagTxSupported	Tx Adaptive Input Eq Fail Flags not supported/supported, Tx CDR Loss of Lock Flags not supported/supported, Tx Loss of Signal Flags not supported/supported, Tx Fault Flags not supported/supported.
158	CDRLOLFlagRxSupported, LOSFlagRxSupported	Rx CDR Loss of Lock Flags not supported/supported, Rx Loss of Signal Flags not supported/supported.
161	TxInputEqRecallBuffersSupported, TxInputEqFreezeSupported, TxInputAdaptiveEqSupported, TxInputEqFixedManualControlSupported, TxCDRBypassControlSupported, TxCDRSupported	Tx Input Eq Store/Recall not supported/buffer counter = 1/2, Tx Input Eq Freeze not supported/supported, Adaptive Tx Input Eq not supported/supported, Tx Input Eq Fixed Manual control not supported/supported, If a Tx CDR is supported, it cannot/can be bypassed, Tx CDR not supported/supported

Byte	Summary	Description
162	StagedSet1Supported, RxOutputEqControlSupported, RxOutputAmplitudeControlSupported, RxCDRBypassControlSupported, RxCDRSupported	Staged Control Set 1 supported on Page 10H, Rx Output Eq control not supported/Pre-cursor control supported/Post-cursor control supported/Pre- and Post-cursor control supported
163	CdbInstancesSupported, CdbBackgroundModeSupported, CdbAutoPagingSupported, CdbMaxPagesEPL	CDB functionality not supported/One or two instance supported, Background CDB operation not supported/supported, Auto Paging and Auto Page wrap not supported/supported, The EPL Page range supported or, equivalently, the maximum length of extended payload.
164	CdbReadWriteLengthExtension	CdbReadWriteLengthExtension = i specifies i*8 allowable additional number of bytes in a WRITE or READ access to an EPL
165	CdbCommandTriggerMethod, CdbExtMaxBusyTime	Determines how the host triggers CDB command processing in the module and when this occurs, CdbExtMaxBusyTime = X encodes the maximum CDB busy time TCDBB as max(1,X)*160 ms in a range of 160 ms to 4960 ms.
166	CdbMaxBusySpecMethod, CdbMaxBusyTime	Indicates that the maximum CDB busy time TCDBB is specified via CdbMaxBusyTime or CdbExtMaxBusyTime CdbMaxBusyTime = X encodes the maximum CDB busy time TCDBB as (80–max(80,X)) ms in a range of 0 ms to 80 ms.
167	MaxDurationModulePwrDn, MaxDurationModulePwrUp	Encoded maximum duration of the ModulePwrDn/ModulePwrUp state
168	MaxDurationDPTxTurnOff/On	Encoded maximum duration of the DPTxTurnOff/On state

Table 9-10 Page 10H

Byte	Summary	Description
128	DPDeinitLanes	Data Path initialization control for host lane 1-8
129	InputPolarityFlipTxs	Tx input polarity no flip/flip for lane 1-8
130	OutputDisableTxs	Tx output enabled/disabled for media lane 1-8
131	AutoSquelchDisableTxs	Automatic Tx output squelching function disabled for

Byte	Summary	Description
		media lane 1-8
132	OutputSquelchForceTxs	Tx output squelched/no impact for media lane 1-8
134	AdaptiveInputEqFreezeTxs	Tx input equalizer adaptation frozen at last value/No impact on Tx input eq adaptation behavior for lane 1-8
135-136	AdaptiveInputEqStoreTxs	Tx Input Equalizer Adaptation Store location for lane 1-8
137	OutputPolarityFlipRxs	Rx output polarity flip/No Rx output polarity flip for lane 1-8
138	OutputDisableRxs	Rx output enabled/disabled for lane 1-8
139	AutoSquelchDisableRxs	Automatic Rx output squelching function enabled/disabled (when supported) for host lane 1-8
143	ApplyDPInitLanes	Trigger the Provision procedure using the Staged Control Set 0 settings for host lane 1-8, with feedback provided in the associated ConfigStatusLane1-8 field.
144	ApplyImmediateLanes	Trigger the Provision or the Provision-and-Commission procedure using the Staged Control Set 0 settings for host lane 1-8, with feedback provided in the associated ConfigStatusLane 1-8 field.
145-152	DPConfigLanes	Staged Control Set 0, Data Path Configuration per Lane
153	AdaptiveInputEqEnableTxs	Staged Control Set 0, Enable/Disable adaptive Tx input equalization.
154-155	AdaptiveInputEqRecallTxs	Staged Control Set 0, Recall stored Tx input equalizer adaptation settings for host lane 1-8 when Staged Control Set is copied to Active
156-159	FixedInputEqTargetTxs	Staged Control Set 0, Manual fixed Tx input equalizer control.
160	CDREnableTxs	Staged Control Set 0, Tx 1-8 CDR enabled/bypassed.
161	CDREnableRxs	Staged Control Set 0, Rx 1-8 CDR enabled/bypassed.
162-165	OutputEqPreCursorTargetRxs	Staged Control Set 0, Rx output equalization pre-cursor target
166-169	OutputEqPostCursorTargetRxs	Staged Control Set 0, Rx1-8 output equalization post-cursor target
170-173	OutputAmplitudeTargetRxs	Staged Control Set 0, Rx 1-8 output amplitude target
178	ApplyDPInitLanes	Trigger the Provision procedure using the Staged Control Set 1 settings for host lane 1-8, with feedback provided in the associated ConfigStatusLane1-8 field.
179	ApplyImmediateLanes	Trigger the Provision or the Provision-and-Commission procedure using the Staged Control Set 1 settings for host lane 1-8, with feedback provided in the associated ConfigStatusLane 1-8 field.

Byte	Summary	Description
180-187	DPConfigLanes	Staged Control Set 1, Data Path Configuration per Lane
188	AdaptiveInputEqEnableTxs	Staged Control Set 1, Enable/Disable adaptive Tx input equalization.
189-190	AdaptiveInputEqRecallTxs	Staged Control Set 1, Recall stored Tx input equalizer adaptation settings for host lane 1-8 when Staged Control Set is copied to Active
191-194	FixedInputEqTargetTxs	Staged Control Set 1, Manual fixed Tx input equalizer control.
195	CDREnableTxs	Staged Control Set 1, Tx 1-8 CDR enabled/bypassed.
196	CDREnableRxs	Staged Control Set 1, Rx 1-8 CDR enabled/bypassed.
197-200	OutputEqPreCursorTargetRxs	Staged Control Set 1, Rx output equalization pre-cursor target
201-204	OutputEqPostCursorTargetRxs	Staged Control Set 1, Rx1-8 output equalization post-cursor target
205-208	OutputAmplitudeTargetRxs	Staged Control Set 1, Rx 1-8 output amplitude target

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Byte	Summary	Description
206-213	DPConfigLanes	Active Control Set, Data Path Configuration
217-220	FixedInputEqTargetTxs	Active Control Set, FixedInputEqTargetTx1-8
221	CDREnableTxs	Active Control Set, CDR enabled/bypassed
222	CDREnableRxs	Active Control Set, Rx 1-8 CDR enabled/bypassed.
223-226	OutputEqPreCursorTargetRxs	Active Control Set, Rx output equalization pre-cursor target
227-230	OutputEqPostCursorTargetRxs	Active Control Set, Rx1-8 output equalization post-cursor target
231-234	OutputAmplitudeTargetRxs	Active Control Set, Rx 1-8 output amplitude target

Table 9-12 Page 9FH

Byte	Summary	Description
128-129	CMDID	U16 CDB Command Code (CMDID) identifies a CDB command to be executed and writing this field also "sends" the CMD message from host to module for processing.
130-131	EPLLength	U16 Extended Payload Length (EPLLength) specifies the host-written number of command message body bytes in EPL, in Pages A0h-AFh. Valid lengths are 0-2048.
132	LPLLength	U8 Local Payload Length (LPLLength) specifies the host-written number of command message body bytes in LPL, on this Page 9FH.

Byte	Summary	Description
133	CdbChkCode	U8 CDB Check Code (CdbChkCode) is computed by the host as the one's complement of the arithmetic sum of Bytes 9Fh:128 to 9Fh:(136+LPLLength-1) excluding Bytes 9Fh:133-135.
134	RPLLength	U8 REPLY Payload Length (RPLLength) is computed by the module and encodes the length of REPLY data returned.
135	RPLChkCode	U8 REPLY Payload Check Code (RPLChkCode) is computed by the module
136-255	LPL	Local Payload (LPL): Message body area sufficient for lengths not exceeding 120 bytes for host-written CMD data or module-written REPLY data (possibly overwriting CMD data).

Note: CMDIDs 0000h, 0001h, 0002h, 0040h, 0041h, 0042h, 0100h, 0101h, 0103h, 0104h, 0107h, 0109h, and 010Ah should be tested.

10 Interconnection and Interworking

The clause is organized into several methods for the industry to reference in interoperable and interconnect testing.

10.1 Receiver Sensitivity Test Under Interworking

10.1.1 Definition

The ‘**receiver sensitivity test under interworking’** is defined as the minimum average optical power per lane under interworking when the specified BER of the optical module is met at the specified modulation rate. The unit is dBm.

10.1.2 Block Diagram

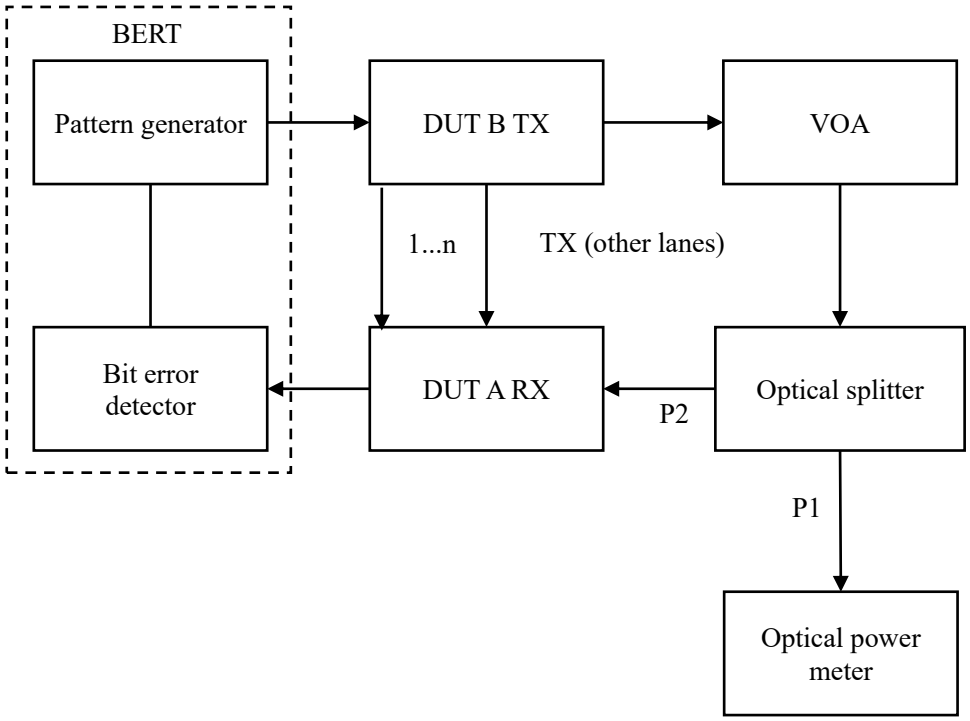

Figure 10-1 Receiver sensitivity test under interworking test

10.1.3 Test Steps

a. Connect the test system according to Figure 10-1.

b. Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6 2.

c. When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d. Measure the optical power values of the two output ports of the **Optical splitter** to P1 and P2 defined in Figure 10-1. Determine the optical power compensation value using the following equation: ΔP = P2 – P1. Then the receive optical power(P2) of the DUT can be calculated as P2=P1+ΔP.

e. Adjust the optical attenuator to 0 dB and wait for a time interval. After confirming the phase lock of the **BERT**, wait until the BER is stable. Then record the BER after 3 seconds.

f. Note:

Calculate the time interval of error bits accumulation when the is BER tested based on confidence (95%), BER (2.4E-4), and the following equation:

Equation 10-1:

Where: $CL = 1 - e^{-N_{bits} \bullet BER}$

CL: confidence.

N_{bits}: bits accumulation that the pattern generator sends in the time interval.

BER: bit error ratio.

The time interval of error bits accumulation is 2.35E-7s when CL is 95% and the BER is 2.4E-4. The test duration is 3 seconds.

g. Adjust the attenuation value of the **VOA** until the measured BER is around BER 1E-6.

Note: The step of adjusting the attenuation value is advised to be set at 0.5dB.

h. Adjust the attenuation value of the **VOA** until the measured BER rests stably 2.4E-4.

Note: The step of adjusting the attenuation value is advised to be set at 0.1dB.

i. The above receive optical power and the corresponding BER are drawn as a BER curve, according to which the received optical power corresponding to the target BER is obtained, namely, the 'receiver sensitivity'.

j. When for a multi-lane optical module, repeat the test for other lanes.

10.2 FEC Capability Test Under Interworking

10.2.1 Definition

For optical modules with the built-in FEC function, verify correctable BER limit under interworking. For optical modules without built-in FEC function, verify correctable BER limit using the host under interworking.

10.2.2 Block Diagram

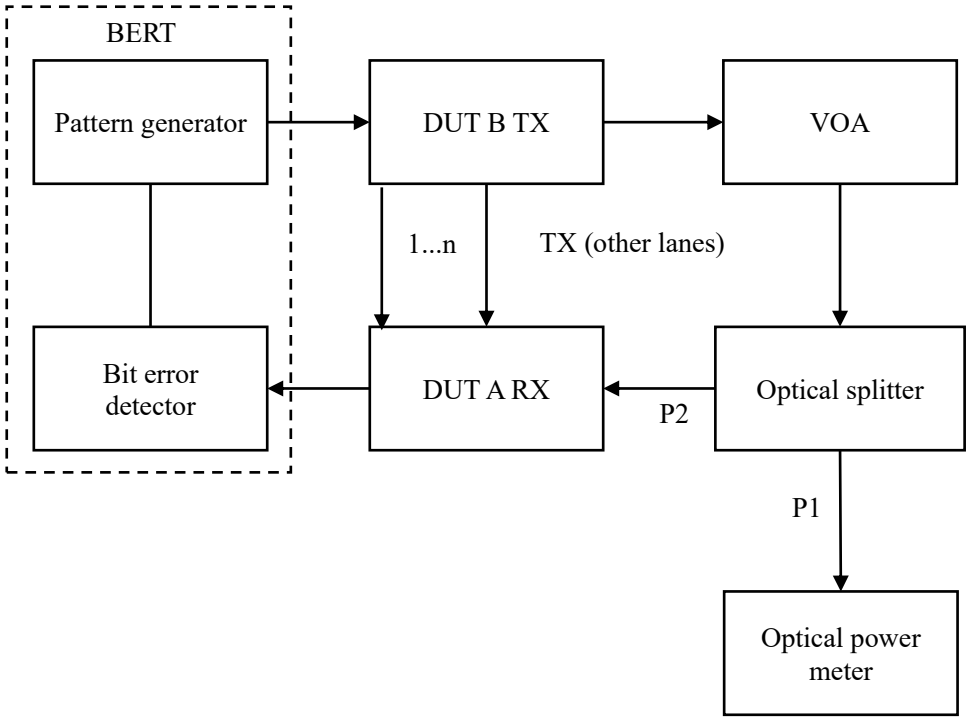

Figure 10-2 FEC capability test under interworking test

10.2.3 Test Steps

a Connect the test system according to Figure 10-2.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6 2.

c Record the bit error distribution.

d Adjust the attenuator value of the **VOA** to gradually reduce the optical power received by the optical module, until the bit error detected by the **BERT** disappears.

Note: It is recommended that the adjustment step of the attenuator be set to 0.5 dB and that when receiver optical power approaches the receiver sensitivity limit, the adjustment step of the attenuator be set to 0.1dB.

e Check the performance of the optical module, record the BER before correction and the bit error distribution.

10.3 Receive Overload Power Test Under Interworking

10.3.1 Definition

The receive overload power test under interworking is defined as the maximum average optical power per lane under interworking when the specified BER of optical module is met at the specified modulation rate. The unit is dBm.

10.3.2 Block Diagram

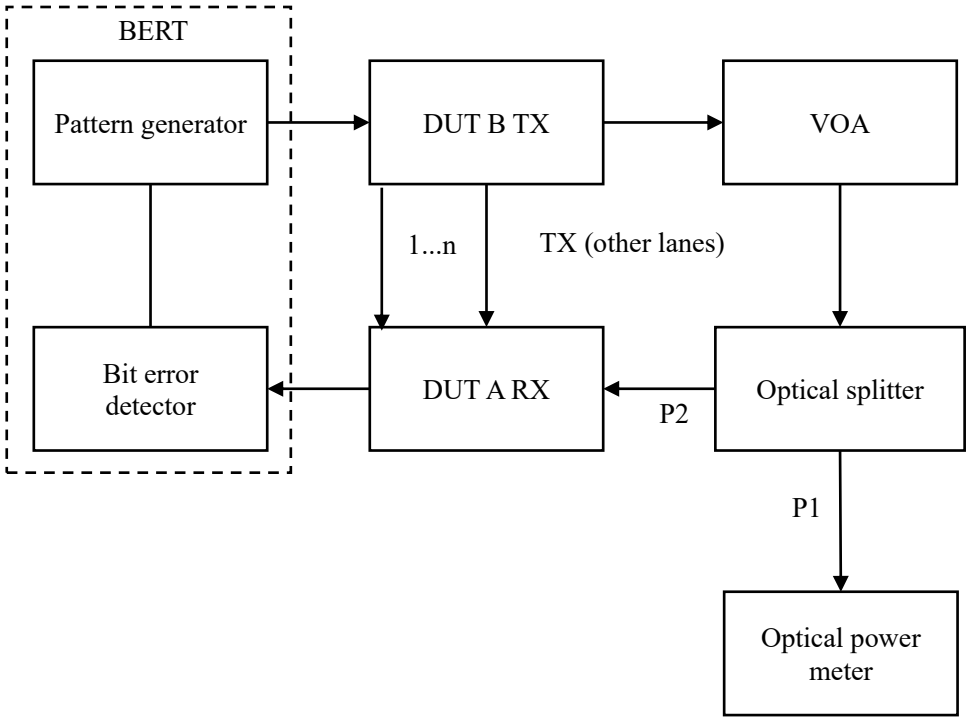

Figure 10-3 Overload optical power test under interworking test

10.3.3 Test Steps

a Connect the test system according to Figure 10-3.

b Set the output service rate, modulation format, amplitude, test pattern and other parameters for the **BERT** based on the characteristics of the optical module. Use the test pattern defined in Table 6 2.

c When for a multi-lane optical module, ensure that each optical lane is tested individually by connecting to an external wavelength demultiplexer and all other lanes are in operation using the same test pattern.

d Adjust the attenuator value of the **VOA** to gradually reduce the optical power received by optical module, until the bit rate detected by the **BERT** increases to the specified value.

Note: The power should not exceed the optical power damage threshold of the optical module.

e Read the optical power of the measured lane.

f When for a multi-lane optical module, repeat the test for other lanes.

11 References

[1] YD/T 2798.2-2020 Measurement Method of Optical Transceiver for Optical Communications – Part2: Muti-wavelength.

[2] IEEE 802.3bs-2017 Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200Gb/s and 400Gb/s Operation.

[3] IEEE 802.3cu-2021 Amendment 11: Physical Layers and Management Parameters for 100Gb/s and 400Gb/s Operation over Single-Mode Fiber at 100Gb/s per wavelength.

[4] IEEE Std 802.3™ -2018: Standard for Ethernet.

[5] OIF-CEI-05.0: Common Management Interface Specification

[6] IEC 61280-1-1: Fibre Optic Communication Subsystem Basic Test Procedures Part 1-1: Test Procedures for General Communication Subsystems -Transmitter Output Optical Power Measurement for Single-mode Optical Fibre Cable

[7] IEC 61280-1-3: Fibre Optic Communication Subsystem test procedures – Part1-3: General Communication Subsystems – Measurement of central wavelength, spectral width and additional spectral

[8] SFF-8679: Reversion 1.8 QSFP+ 4X Hardware and Electrical Specification

[9] SFF-8636: Rev 2.10a Management Interface for 4-lane Modules and Cables

[10] QSFP-DD Hardware Specification Rev5.1: QSFP-DD Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER