International Photonics & Electronics Committee

OIO Pluggable External Laser Source (PELS) Implementation Agreement

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OIO Pluggable External Laser Source (PELS) Implementation Agreement

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OIO Pluggable External Laser Source (PELS) Implementation Agreement

ABSTRACT

This implementation agreement defines a compact form factor with blindmated electro-optical interface for pluggable external laser source in optical input/output applications.

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1 Introduction

1.1 OIO Application Diagram

As bandwidth demands increase, the capacities of optical modules and switch ASICs have both increased rapidly in the past decade. However, the development of pluggable optical module has encountered great challenges due to large-bandwidth, high-density, low-power, and cost-efficient requirements. OIO (optical Input/Output) technology is an approach using large-bandwidth and high-density optical interfaces to solve the I/O fan-out of large-capacity chips such as switch ASICs, CPUs, and GPUs.

At present, the application of OIO technology in switches needs to be achieved through the combination of optical engines (OE) and laser source. An illustrative diagram of OIO application is shown in Figure 1.1, in which, for example, a 51.2 Tb/s switch consists of an ASIC chip, 16 OEs, and 16 PELSs. Each OE transmits 3.2Tb/s with a total of 32 LD/Rx lanes and provides optical I/O to the switch ASIC via optical connections. The external laser source (ELS) produces a continue wavelength (CW) laser light for OE to convert the electrical signal output from ASIC into an optical signal through the external modulation solutions. With OE silicon split ratio of 1:4, and each PELS contains 8 lasers, a PELS can provide laser source to a 3.2 Tb/s (4*8*100 Gb/s) OE. By applying OIO technology to switches with shorter electrical link from ASICs to OE, one can expect signal quality and bandwidth improvement as well as power consumption reduction.

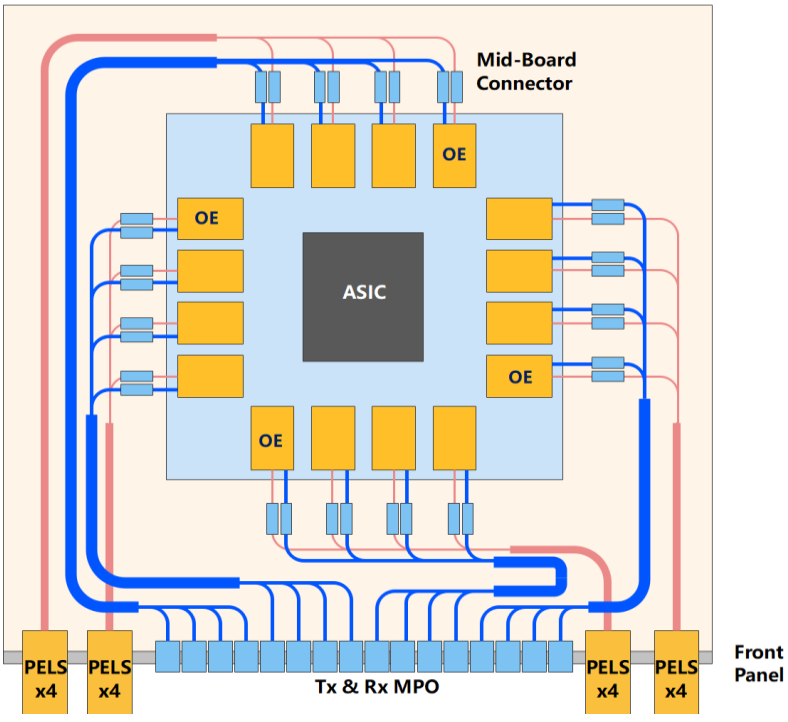


Figure 1.1 Illustrative Diagram of OIO Application

The laser source of OIO technology is solved by two methods: one is to use an external laser source to provide a non-modulated laser, the other is integrated laser diodes on silicon photonics chip. For integrated laser diode solutions, the integration of lasers and ASIC chips on the same board can improve the integration, but the lasers will

be suffered by critical environment and need to have a backup laser in order to ensure adequate reliability. In the external laser solution, ELS can be divided into two types: pluggable external laser source (PELS) and on-board external laser source. The on-board external laser source is directly set into the switch. Compared with integrated laser diodes, this solution is more mature. In addition, the optical connection between the laser and the ASIC can be fixed in the switch, reducing the optical connection interface loss. However, similar to the integrated laser diodes on silicon photonics chip, this solution cannot replace the laser alone. It also requires a backup. The pluggable external laser source solution provides a laser source for the switch through the front panel like a pluggable optical module. The switch realizes the drive and optical connection through the specific electro-optical connection port. Three technical solutions are shown in Figure 1.2. PELS has a good heat dissipation environment, so the temperature is the lowest. The integrated silicon laser and the chip are on the same PCB, which requires additional heat dissipation, so the temperature is the highest. Generally, PELS has advantages in reliability, operability, maintainability, serviceability and stability.

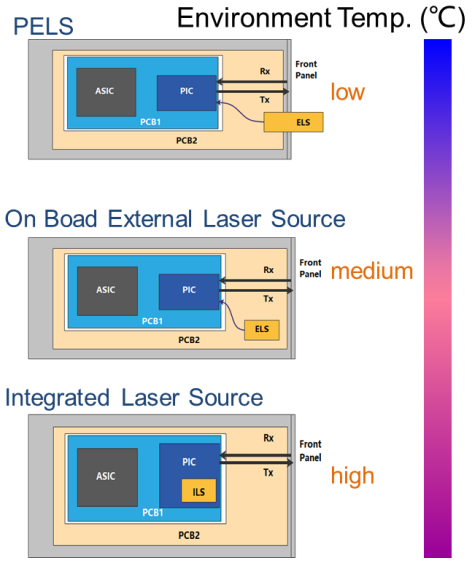


Figure 1.2 Three solutions of source and its environment temperature.

1.2 Pluggable External Laser Source (PELS)

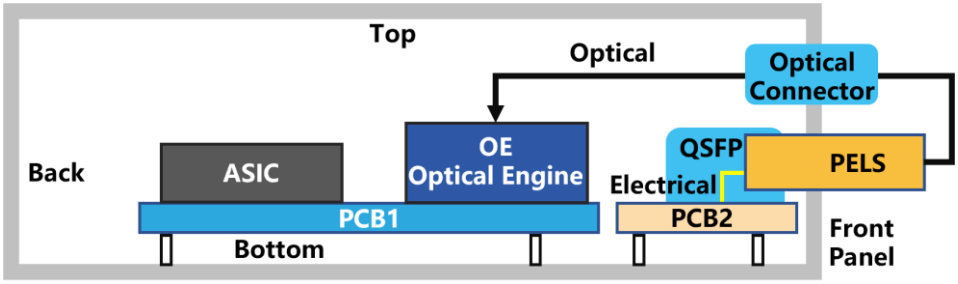


Figure 1.3 Concept of PELS with QSFP like and Optical Connector on the both sides

The pluggable external laser source would use QSFP form factor dimensions, and the non-modulated laser can be re-connected to the switch using the front panel, as shown in Figure 1.3. One PELS requires two ports to operate

under this method, making the front panel very crowded or over size. And the additional interface loss introduced by the reconnection will also reduce the performance and reliability of the PELS.

Since the output optical power of the external laser is much larger than pluggable optical module, for laser safety consideration, the electrical-optical (E/O) connector of PELS should be designed on the same side (toward the switch), as shown in Figure 1.4. In this solution, the electrical interface and optical interface are set at the same side. So, a new interface specification needs to be adopted to support the electro-optical interface. Since the connector is inside the switch, and the optical interface and the electrical interface are made in the same interface, the cleaning of the interface (especially the optical interface) will become very complicated and difficult. The factors for design should include both break-out or wave-fusion applications, power of each wavelength, number of fibers, connector type, fiber separation and arrangement.

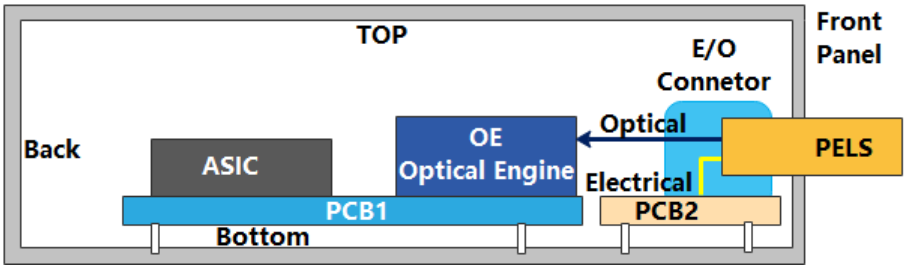


Figure 1.4 Concept of PELS with Electrical/Optical Connector on the same side

The main function of PELS is to provide a stable, high-quality, narrow linewidth (~MHz) laser source for the OE. PELS has multiple lasers to achieve simultaneous output of multiple lasers with independently adjustable power. In order to maintain the polarization of the laser, the transmission fiber should use polarization maintaining fiber (PMF). The output laser is connected to the OE through an optical interface, which should be a polarization interface. The electrical interface of PELS provides power for PELS, controls the operation of PELS and regulates the output of optical port through corresponding pins. PELS cannot provide active cooling through the switch. When only passive heat dissipation can be used, the working conditions of multiple high-power lasers inside the PELS will be a huge challenge. The layout of the connectors and PELS modules is also important, as it affects the fiber routing and management inside the switch box. The faceplate configuration requires careful consideration of thermal management, particularly since the CPO switch box could potentially need to dissipate a kW or more.

In order to achieve maximum air flow for better thermal dissipation in the switch box, one possible configuration is to move the optical interface for OE TRx on the front-panel to the PELS module, as described in Figure 1.5, making the PELS act as pass-through module, as described in Figure 1.6.

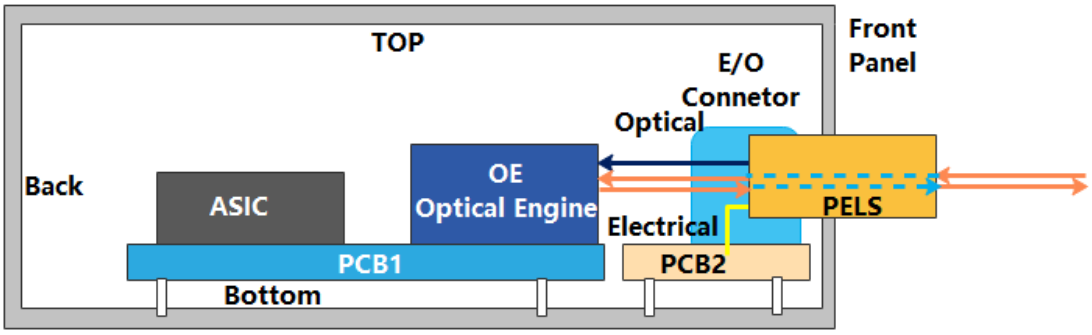


Figure 1.5 Concept of OE TRx optical interface integrated on the PELS module

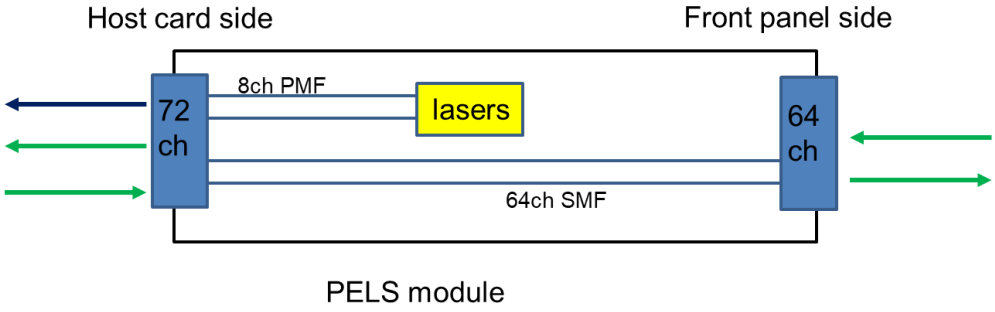


Figure 1.6 Concept of pass-through PELS module

1.3 Scope

This document provides specifications on the requirements for a pluggable external laser source designed for network equipment applications using co-packaged optics (CPO), near-packaged optics (NPO) and optical input and output (OIO) .

2 Mechanical Specifications

2.1 Mechanical Overview

Figure 2.1 gives the mechanical overview of the OIO PELS, which consists of following components:

Part A: main body of OIO PELS module;

Part B: PCB towards to the host side, to connect to the host side electrical connector;

Part C: Optical holder towards to the host side, to connect to the host side optical connector;

Part D: MT ferrule within the optical holder, also towards to the host side, to connect to host side MT fiber interface;

Other parts: unlock mechanics and pull tab, etcs;

A detailed look of the Part B, C and D is given in Figure 2.2.

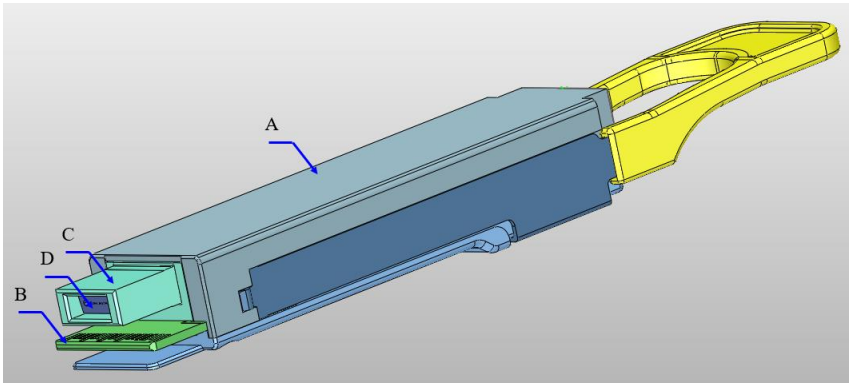


Figure 2.1 Mechanical overview of OIO PELS

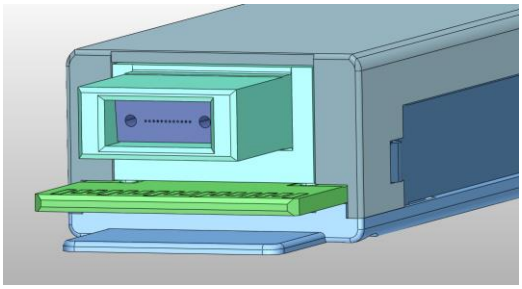


Figure 2.2 Detailed look of OIO PELS

2.2 Mechanical Size

The OIO PELS has two types of mechanical size, similar to QSFP-DD. Figure 2.3 gives the detailed size parameters of type-A OIO PELS. Figure 2.4 gives the size parameters of optical and electrical interfaces of OIO PELS, which works for both type-A and type-B OIO PELS.

Dimension	Size	Note
Width (mm)	18.35	
Height (mm)	11.05	
Length (mm)	77.65 (type-A) 92.65 (type-B)	this length does NOT include the length of pull-tab and the heatsink of the IHS as described in Section 6.

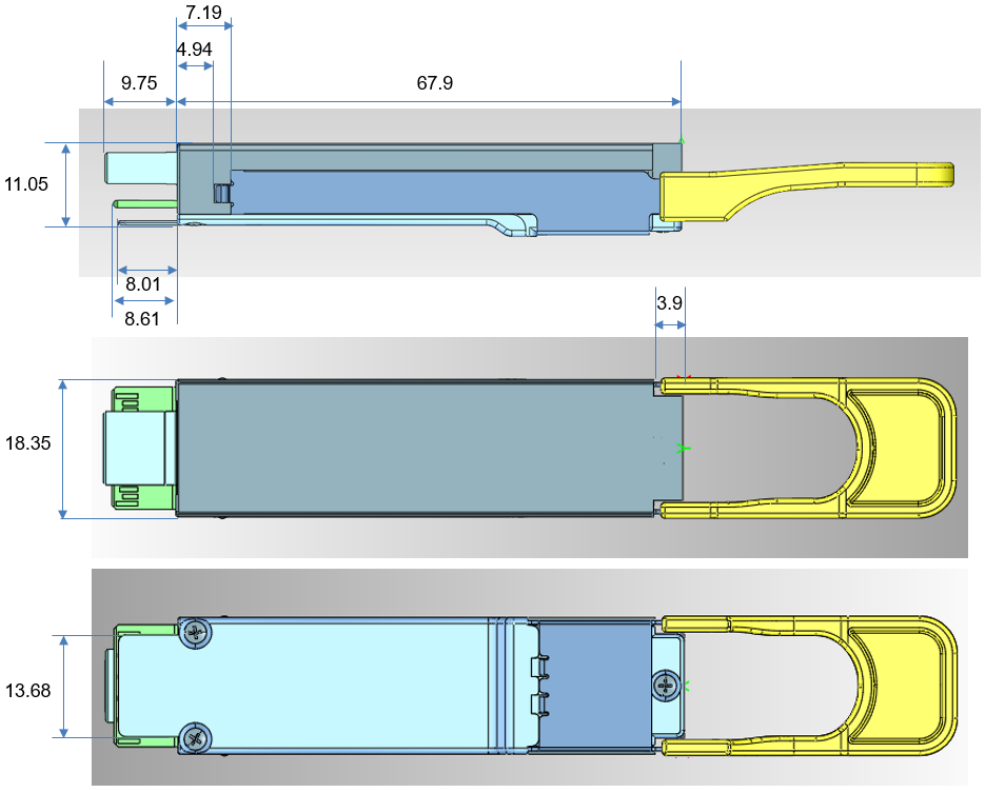


Figure 2.3 Detailed size parameters of type-A OIO PELS

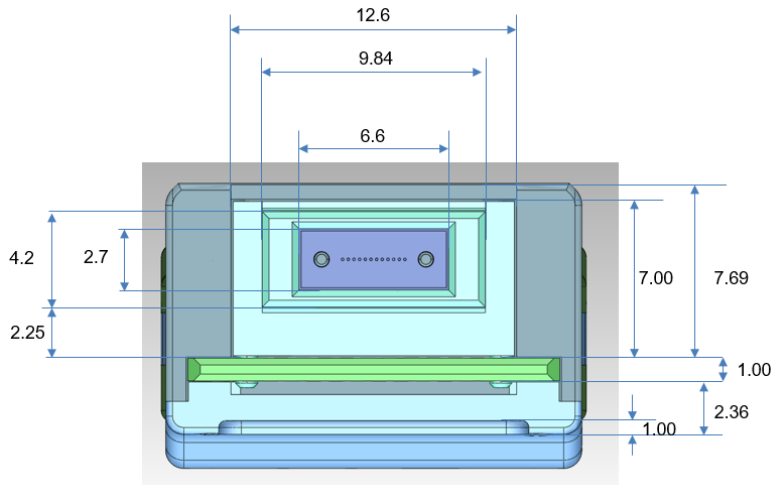


Figure 2.4 Detailed size parameters of optical and electrical interfaces of OIO PELS

3 Optical Specifications

3.1 MT connector type, Channel number and Optical Port Map

The position fiber naming and assignment are defined in Figure 3.1 and Figure 3.2. Unused channels of the MT-12 and the MT-16 must be filled with dummy fibers to prevent contamination or possible damage when falsely mating for example an 8 fiber, 12 fiber and 16 fiber MT ferrule. Table 3-1, Table 3-2 and Table 3-3 give the assignment of wavelengths for 1311 (DR Type) and CWDM4 (FR Type) type modules relative to the fiber position. 8PMF per MT-12, 12PMF per MT-12 and 16PMF per MT-16 ferrule configurations are specified.

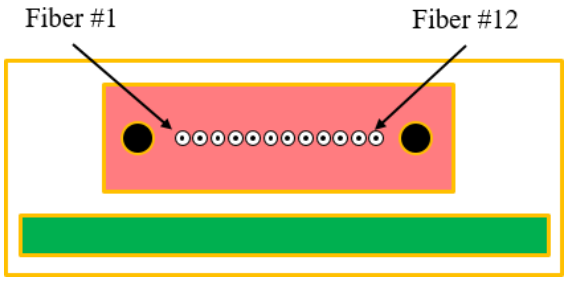


Figure 3.1 PELS MT-12 Ferrule output endface for 12ch optical channel

Table 3-1 MT-12 optical port map for 8PMF

Position	Symbol	DR Type 1	DR Type 2	FR Type
Fiber #1	L0	Laser0, 1311nm	Not Used	Laser0, 1271nm
Fiber #2	L1	Laser1, 1311nm	Not Used	Laser1, 1291nm
Fiber #3	L2	Laser2, 1311nm	Laser0, 1311nm	Laser2, 1311nm
Fiber #4	L3	Laser3, 1311nm	Laser1, 1311nm	Laser3, 1331nm

Fiber #5	NC	Not Used	Laser2, 1311nm	Not Used
Fiber #6	NC	Not Used	Laser3, 1311nm	Not Used
Fiber #7	NC	Not Used	Laser4, 1311nm	Not Used
Fiber #8	NC	Not Used	Laser5, 1311nm	Not Used
Fiber #9	L4	Laser4, 1311nm	Laser6, 1311nm	Laser4, 1271nm
Fiber #10	L5	Laser5, 1311nm	Laser7, 1311nm	Laser5, 1291nm
Fiber #11	L6	Laser6, 1311nm	Not Used	Laser6, 1311nm
Fiber #12	L7	Laser7, 1311nm	Not Used	Laser7, 1331nm

Table 3-2 MT-12 optical port map for 12PMF

Position	Symbol	DR Type	FR Type
Fiber #1	L0	Laser0, 1311nm	Laser0, 1271nm
Fiber #2	L1	Laser1, 1311nm	Laser1, 1291nm
Fiber #3	L2	Laser2, 1311nm	Laser2, 1311nm
Fiber #4	L3	Laser3, 1311nm	Laser3, 1331nm
Fiber #5	L4	Laser4, 1311nm	Laser4, 1271nm
Fiber #6	L5	Laser5, 1311nm	Laser5, 1291nm
Fiber #7	L6	Laser6, 1311nm	Laser6, 1311nm
Fiber #8	L7	Laser7, 1311nm	Laser7, 1331nm
Fiber #9	L8	Laser8, 1311nm	Laser8, 1271nm
Fiber #10	L9	Laser9, 1311nm	Laser9, 1291nm
Fiber #11	L10	Laser10, 1311nm	Laser10, 1311nm
Fiber #12	L11	Laser11, 1311nm	Laser11, 1331nm

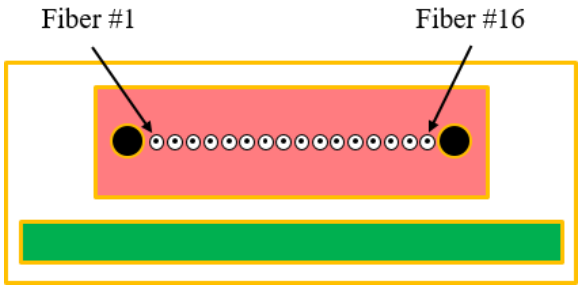


Figure 3.2 PELS MT-16 Ferrule output endface for 16ch optical channel

Table 3-3 MT-16 optical port map for 16PMF

Position	Symbol	DR Type	FR Type
Fiber #1	L0	Laser0, 1311nm	Laser0, 1271nm
Fiber #2	L1	Laser1, 1311nm	Laser1, 1291nm
Fiber #3	L2	Laser2, 1311nm	Laser2, 1311nm
Fiber #4	L3	Laser3, 1311nm	Laser3, 1331nm
Fiber #5	L4	Laser4, 1311nm	Laser4, 1271nm
Fiber #6	L5	Laser5, 1311nm	Laser5, 1291nm
Fiber #7	L6	Laser6, 1311nm	Laser6, 1311nm
Fiber #8	L7	Laser7, 1311nm	Laser7, 1331nm
Fiber #9	L8	Laser8, 1311nm	Laser8, 1271nm
Fiber #10	L9	Laser9, 1311nm	Laser9, 1291nm
Fiber #11	L10	Laser10, 1311nm	Laser10, 1311nm
Fiber #12	L11	Laser11, 1311nm	Laser11, 1331nm
Fiber #13	L12	Laser12, 1311nm	Laser12, 1271nm
Fiber #14	L13	Laser13, 1311nm	Laser13, 1291nm
Fiber #15	L14	Laser14, 1311nm	Laser14, 1311nm
Fiber #16	L15	Laser15, 1311nm	Laser15, 1331nm

3.2 PELS for pass-through application

For pass-through application described in Figure 1.5, the PELS IA defines the optical interface as Figure 3.3.

For the host card side, a total 72 channel MT is needed for both 8 channel laser output and 64 channels Tx/Rx signal of OE. Two thin MT36 are stacked into an equivalent 72 channel MT. The thin MT36 has 3 rows with 12 channels in each row.

For the front panel side, a total 64 channel MT is needed for Tx/Rx signal of OE. Two possible configurations are illustrated in Figure 3.3. The first configuration is using only 64 channels of an equivalent 72 channel MT stacked by two thin MT36. The thin MT36 has 3 rows with 12 channels in each row. The second configuration is using an equivalent 64 channel MT stacked by two thin MT32. The thin MT32 has 2 rows with 16 channels in each row.

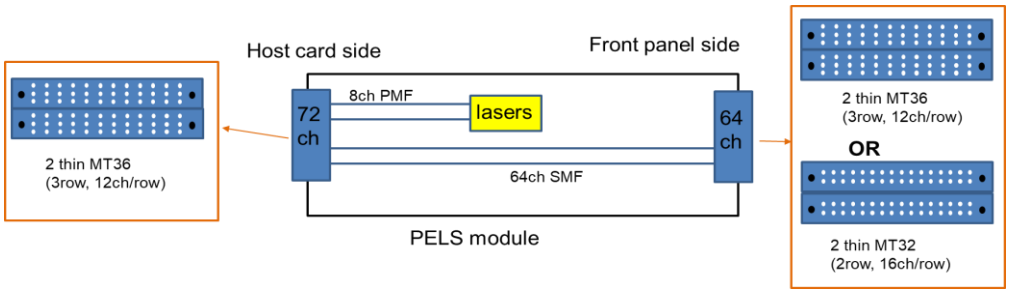


Figure 3.3 PELS with Pass-through design

3.3 PELS Optical Power Range

The optical specifications for the PELS module are given in Table 3-4.

Table 3-4 PELS optical specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
FR4 center wavelength 1	FR-WL1	1264.5	1271	1277.5	nm	
FR4 center wavelength 2	FR-WL2	1284.5	1291	1297.5	nm	
FR4 center wavelength 3	FR-WL3	1304.5	1311	1317.5	nm	
FR4 center wavelength 4	FR-WL4	1324.5	1331	1337.5	nm	
DR4 center wavelength	DR-WL	1304.5	1311	1317.5	nm	
Optical power capability per fiber for 12ch		17.5		19	dBm	
Optical power capability per fiber (1:4 split)		19			dBm	
Minimum set point of operating power per fiber (1:4 split)				15	dBm	
Optical power capability per fiber (1:8 split)		22			dBm	
Minimum set point of operating power per fiber (1:8 split)				18	dBm	
Optical power capability per fiber (1:16 split)		TBD			dBm	
Minimum set point of operating power per fiber (1:16 split)				TBD	dBm	
Laser RIN (Relative Intensity Noise)	RIN	-141.5			dB/Hz	
Laser SMSR	SMSR	30			dB	
Laser linewidth	Δv			2	MHz	
Polarization	r_{ex}	10			dB	TBD

Extinction Ratio						
Output reflectance	Rx_Ref			-26	dB	
Optical return loss tolerance	ORLT			28.2	dB	PELS Optical return loss tolerance: maximum of 3 connectors both DR and FR, assumes 8 lasers per 3.2T

3.4 PMF Rotation

For electric field of laser light output of the OIO PELS is defined as horizontal polarization, as illustrated in Figure 3.4. The system supplier can request for a PELS with PMF slow axis either horizontally or vertically aligned based on different PMF links between PELS and OE.

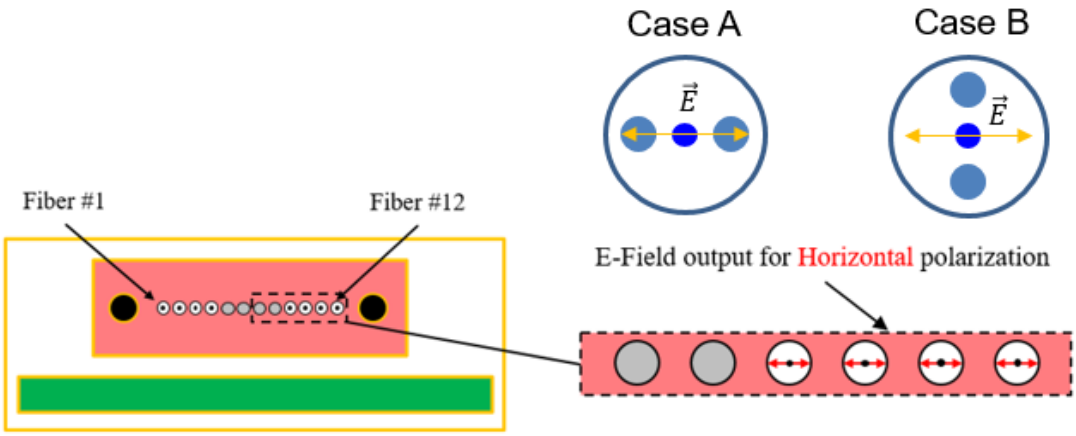


Figure 3.4 Horizontal polarization of OIO PELS. Case A: PMF slow axis horizontally aligned; Case B: PMF slow axis vertically aligned;

4 Electrical Specifications

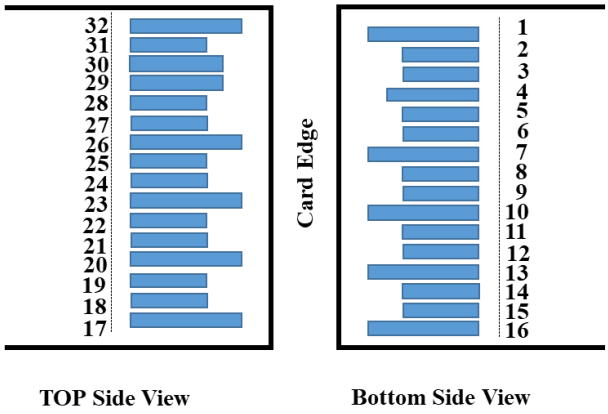
4.1 Electrical Pinout

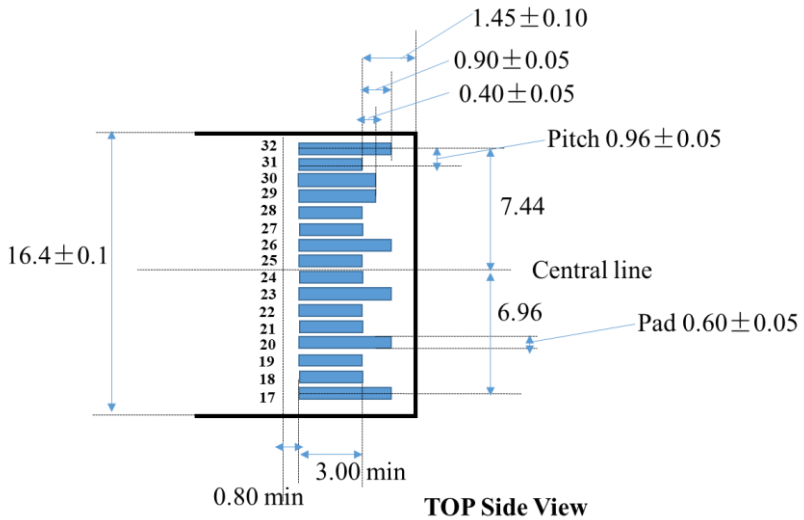
The electrical interface pin definition for the PELS module is shown below in Table 4-1. 32 electrical contacts are included in the host connector to mate to a card edge interface, with corresponding pin layout be given in Figure 4.1. The PELS PCB thickness is nominal 1.0mm.

Table 4-1 PELS Pinout

Pin	Symbol	Description	Requirement	Notes
1	GND LD	Ground LD		
2	Vcc2	LD Power supply	1.5A, +3.3V	
3	Vcc2	LD Power supply	1.5A, +3.3V	
4	Vcc1	Digital Power supply	1.5A, +3.3V	
5	Vcc2	LD Power supply	1.5A, +3.3V	
6	Vcc2	LD Power supply	1.5A, +3.3V	
7	GND LD	Ground LD		
8	ModelSelL	Module Select		
9	ResetL	Module Reset		
10	GND LD	Ground LD		
11	SCL	2-wire serial interface clock		
12	SDA	2-wire serial interface data		
13	DGND	Digital GND		
14	GND TEC	Ground TEC		
15	TBD	Reserved		
16	GND TEC	Ground TEC		
17	Vcc3	Power supply TEC	+3.3V	
18	Vcc3	Power supply TEC	+3.3V	
19	GND TEC	Ground TEC		
20	GND TEC	Ground TEC		
21	Vcc3	Power supply TEC	+3.3V	
22	Vcc3	Power supply TEC	+3.3V	
23	TBD	Reserved		
24	TBD	Reserved		
25	TBD	Reserved		
26	TBD	Reserved		
27	ModPrsL	Module Present		Ground by the module to indicate that the module is present
28	TBD	Reserved		
29	Vcc1	Digital Power supply	1.5A, +3.3V	
30	Vcc1	Digital Power supply	1.5A, +3.3V	
31	LPMode	Low Power Mode		
32	GND LD	Ground LD		

Note that to be determined (TBD) pins have been placed adjacent to the VCC and ground in the event that a future provision is required for additional power and/or ground capacity. Additional notes for each pin are provided in Table 4-1.





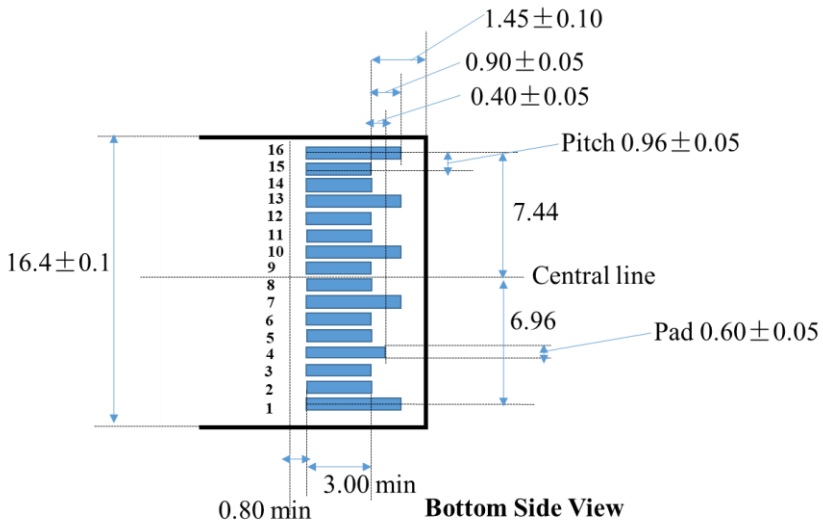


Figure 4.1 Electrical Pin layout view from top and bottom side.

4.2 Power Supplies

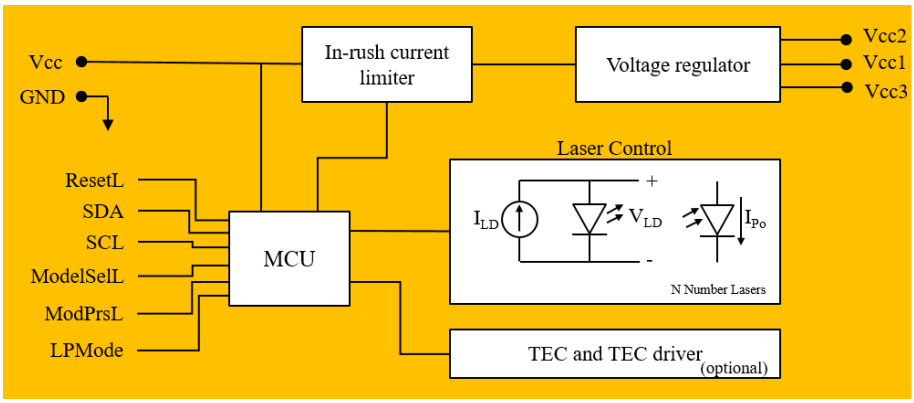


Figure 4.2 Electrical block diagram of a PELS module

Figure 4.2 gives the electrical block diagram of a PELS module. Similar to other CMIS compatible pluggable modules, the ModuleLowPwr state for the PELS module shall represent a minimum electrical power consumption state in order to power the module micro controller unit (MCU) and communicate with the Host. The PELS complies with the CMIS Module State Machine (MSM). When a PELS is initially plugged in the lasers' default state is OFF. First it is in the Resetting state. Upon completion of resetting, it enters the Reset state where it awaits a ResetS = FALSE signal and enters Management Initialization (MgmtInit). Once MgmtInit is complete the PELS enters the ModuleLowPwr or Low Power Mode state. Lasers shall NOT be powered when the PELS module is in LPMode/ModuleLowPwr state. To activate lasers the PELS must transition to the ModuleReady state and receive direction from the Host so as to maximize safety and prevent possible damage to the system or the optical engine. Only the Host Controller may request the Laser to be activated. Further details on management of the PELS are covered in OIF's CMIS Management Implementation Agreement. Additional circuits, such as optional thermo-electric coolers (TECs) can be enabled prior to lasers.

4.3 Power consumption

Power for the PELs shall be delivered by six pairs of 3.3V power and ground pins. The DC current capability of each of these pins is up to 1.5 A with a maximum operating rating DC voltage of 30 V. The total module power consumption of a PELS shall be reported via CMIS using the following optical power classifications in Table 4-2. And the power class of PELS are given in Table 4-3.

Table 4-2 Optical power classes and power consumption

Parameter	Min	Max	Unit	Power consumption
Optical power max per fiber @12ch	17.5	19	dBm	＜9W
Optical power max per fiber 1:4 [DR4]@8ch	19	21	dBm	＜15W
Optical power max per fiber 1:4 [FR4]@8ch	20	22	dBm	＜15W
Optical power max per fiber 1:8 [DR4/FR4]	TBD	TBD	dBm	TBD
Optical power max per fiber 1:4 [DR4]@16ch	TBD	TBD	dBm	TBD
Optical power max per fiber 1:4 [FR4]@16ch	TBD	TBD	dBm	TBD

Table 4-3 Power Class of PELS

Power Class	Max Power(W)	Notes
1	1.5	Low power mode
2	3.5	Consisted with QSFP-DD MSA, Reserved for Advancing Technologies
3	7.0	
4	8.0	
5	9.0	
6	12	Consisted with QSFP-DD MSA
7	15	
8	18	
9	21	
10	>21	TBD for future applications

5 Host side Electrical and Optical Connectors

Followings define the electrical and optical (E/O) connector for the bind-mate application of OIO PELS.

5.1 E/O Connector Mechanical

As shown in Figure 5.1, the OIO PELS solution includes three main components:

A. PELS module (probably with integrated heat sink, which will be described in Section 6;

B. E/O hybrid connector integrated with cage for blind-mate OIO PELS both electrical and optical interface, as shown in Figure 5.1 (2);

C. Host optical connector with clip and spring, as shown in Figure 5.1 (3).

For the E/O hybrid connector integrated with cage shown in Figure 5.1 (2)， further details are given in Figure 5.2.

For the electrical part of the E/O hybrid connector, the electrical female connector is similar to traditional QSFP electrical connector, but with only 32 pins, corresponding to the 32 electrical PCB pins of PELS listed in Table 4-1. The E/O hybrid connector and cage can be press fit on PCB board directly for deployment convenience.

Viewing from the host side, the E/O hybrid connector has a MT adapter for the standard MT ferrule connected to the host OE. Also the MT adapter has two MT alignment slots to align the tiny clip of the host optical connecter, details of which are given in Figure 5.3.

Viewing from the PELS side, the E/O hybrid connector consists of a dust resist door to prevent fiber dust contamination, and reduce the possibility of fiber burning under 17.5~22dBm PELS output optical power.

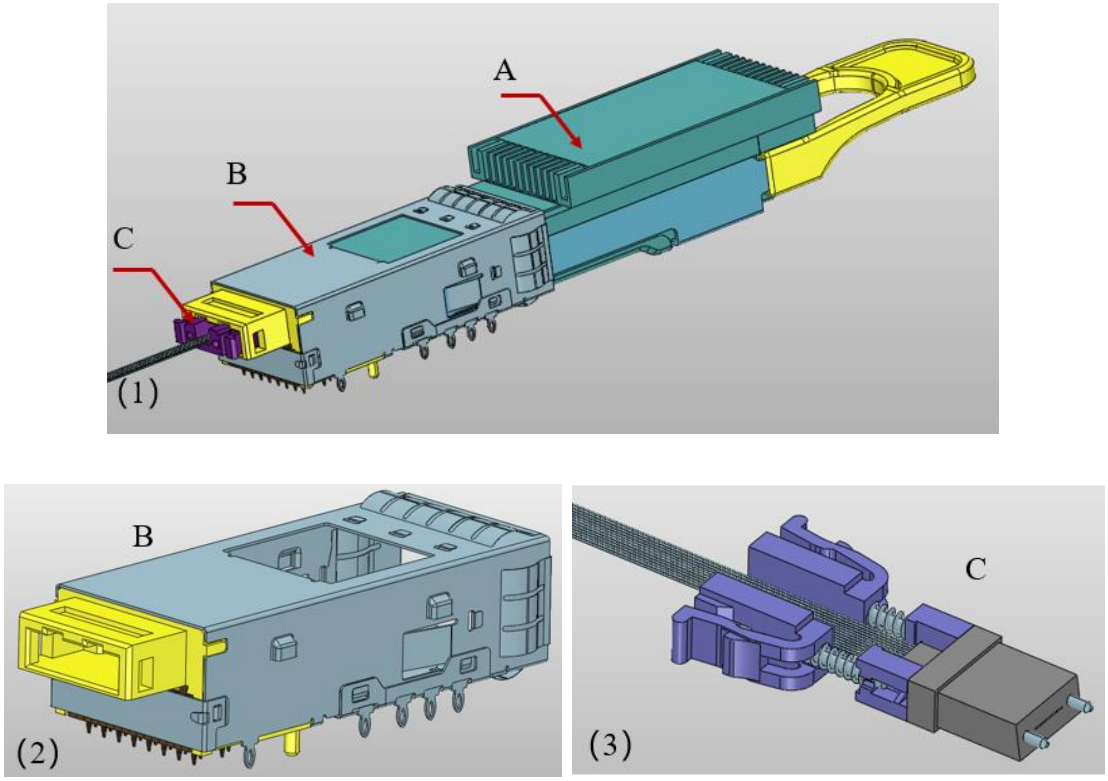


Figure 5.1 OIO PELS solution components overview

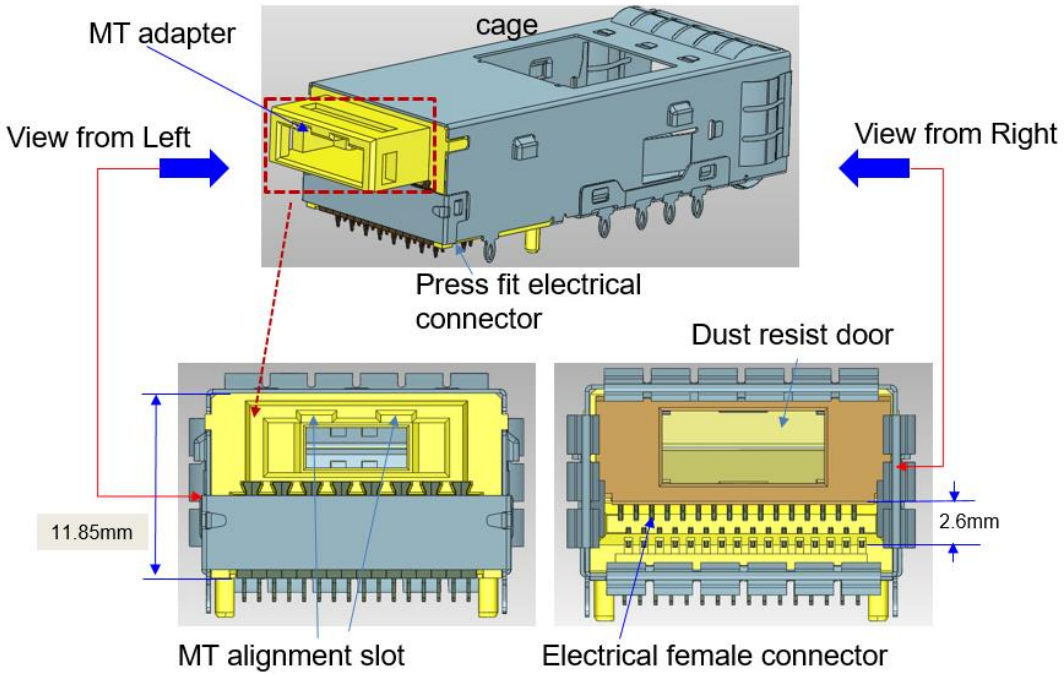


Figure 5.2 Detailed of E/O hybrid connector and cage

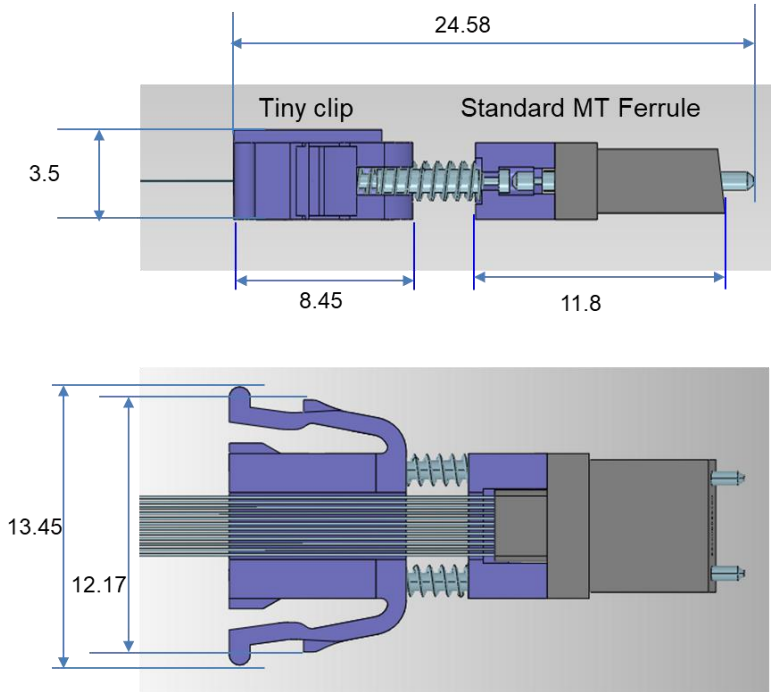


Figure 5.3 Details of host optical connector with clip and spring

The cage is with dimension of Length x Width x Height of 51.56mmx19.25mmx12.16mm, and details are given in Figure 5.4.

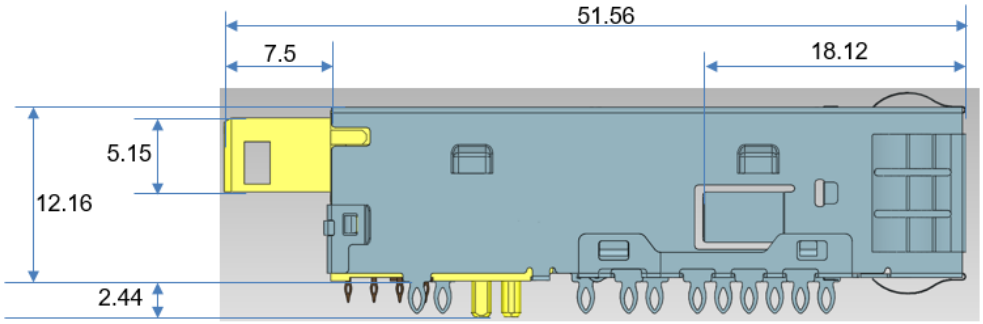


Figure 5.4 Details of host optical connector and cage

5.2 Powered Mate and Demate Sequence

As the PELS with output power around 17.5~22dBm causes permanent damage to MT fiber cores at either host side or module side if the module is plug-in or plug-out in high power state, the module optical connector and host side E/O hybrid connector are designed to avoid fiber burning by ensuring following module mating and demating sequence:

For the mating sequence during the PELS plug-in process:

1) The optical contact between the optical interfaces of PELS and host side MT facet is built first while the electrical contact between the PELS PCB gold fingers and the host side electrical connector is not;

2) Then, as the module plug-in towards to the host side, the electrical connection is built:

Combined with different gold fingers length design of the PELS PCB as described in Figure 4.1 and Table 4-1, the electrical connection is built as following procedures:

a) Firstly, the ground pin electrical contacts are built;

b) Then, the digital power supply Vcc1 electrical contacts are built;

c) Finally, the Vcc2 LD power supply, Vcc3 TEC power supply as well as the low speed electrical pins such as SCL, SDA, ModSelL, ModPrsL, ResetL and LPMode electrical contacts are built.

For the demating sequence during the PELS plug-out process:

1) The electrical contacts are disconnected first while the optical contact between the optical interfaces of PELS and host fiber is still in good connection.

2) Then, as the module plug-out towards to the panel side, the optical contact between the optical interfaces of PELS and host side MT facet is disconnected;

Combined with different gold fingers length design of the PELS PCB as described in Figure 4.1 and Table 4-1, the electrical contacts are disconnected as following procedures:

a) Firstly, the Vcc2 LD power supply, Vcc3 TEC power supply as well as the low speed electrical pins such as SCL, SDA, ModSelL, ModPrsL, ResetL and LPMode electrical contacts are disconnected;

b) Then, the digital power supply Vcc1 electrical contacts are disconnected;

c) Finally, the ground pin electrical contacts are disconnected;

5.3 Belly-to-Belly Design

The E/O hybrid connector and cage is in favor of supporting belly-to-belly deployment. And corresponding host PCB design layout is given in Figure 5.5.

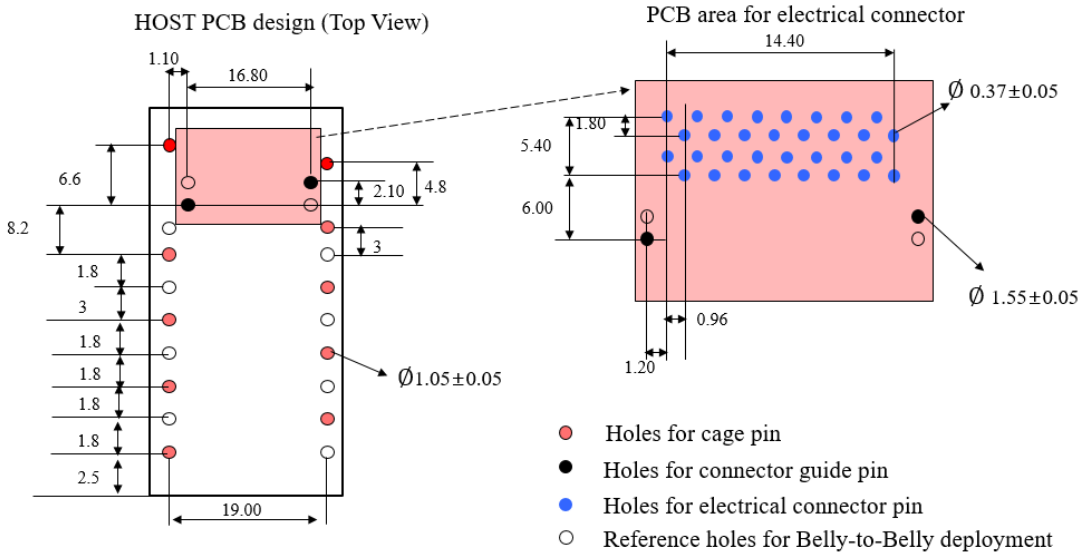


Figure 5.5 Host PCB design layout for PELS belly-to-belly deployment

5.4 Cage Riding Heatsink Dimensions

As shown in Figure 5.1 and Figure 5.2, there is an opening on the top side of the cage, through which cage riding heatsink can be added accordingly for better thermal dissipation. As for the dimensions of cage riding heatsink, system vendors can also design accordingly.

6 Thermal Specifications

6.1 Integrated Heatsink Dimensions

This OIO PELS IA provides following integrated heatsink (IHS) types, as shown in Figure 6.1, module and system vendors can choose corresponding IHS type according to the thermal dissipation management and OIO system faceplate layout. With following IHS, the PELS is expected to support thermal dissipation of different power classes listed in Table 4-3.

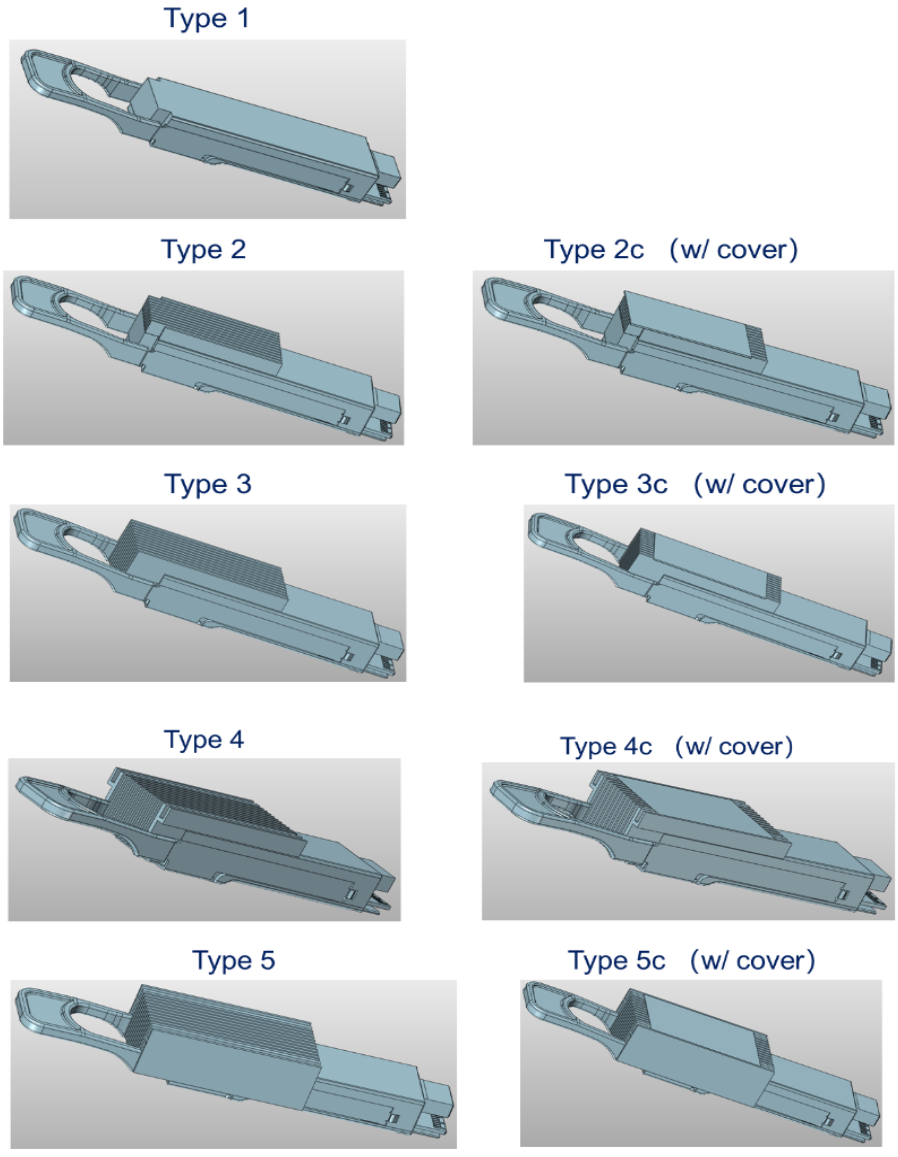


Figure 6.1 Different types of IHS of OIO PELS

6.1.1 PELS with Type 2/2c IHS

Figure 6.2 describes the PELS with top side IHS, naming Type 2 IHS and Type 2c IHS for OIO PELS module without and with top side cover, respectively, and Table 6-1 give suggested IHS size parameters.

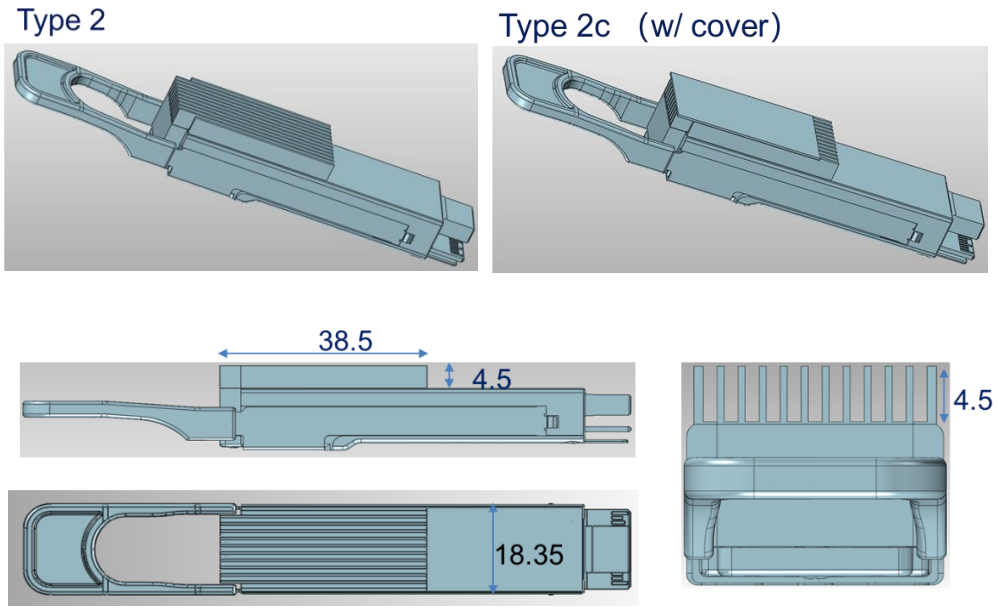


Figure 6.2 Type 2/2c IHS of OIO PELS

Table 6-1 Suggested size parameters of Type 2/2c IHS

IHS Size	**Parameters (mm)**	**Note**
Height	4.5	
Length	38.5	
Fin Total Width	18.35	
Fins Thickness	0.5	Suggested parameters, could be adjusted with applications
Fin Pitch	1.5	
Fin Number	12	
Cover Size (Type 2c only)	≤38.5x18.35	

6.1.2 PELS with Type 3/3c IHS

Type 3/3c IHS = Type 2/2c IHS+ backside IHS

Figure 6.3 describes the PELS with top side IHS, naming Type 3 IHS and Type 3c IHS for OIO PELS module without and with top side cover, respectively, and Table 6-2 give suggested IHS size parameters.

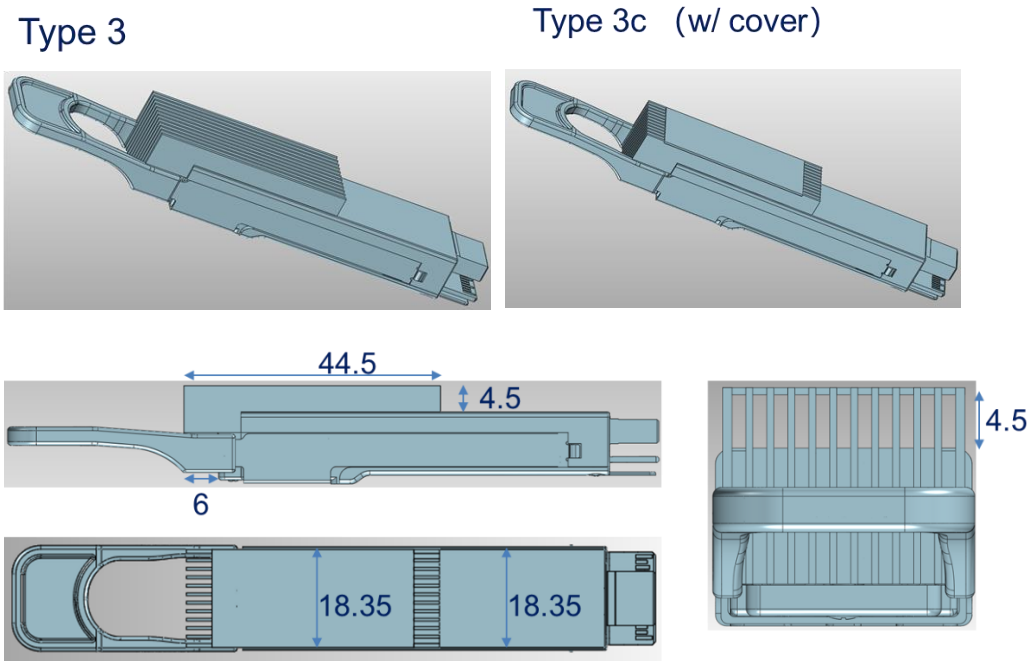


Figure 6.3 Type 3/3c IHS of OIO PELS

Table 6-2 Suggested size parameters of Type 3/3c IHS

IHS Size	**Parameters (mm)**	**Note**
Height	4.5	
Length	44.5	Backside heatsink included
Fin Total Width	18.35	
Fins Thickness	0.5	Suggested parameters, could be adjusted with applications
Fin Pitch	1.5	
Fin Number	12	
Cover Size (Type 3c only)	≤44.5x18.35	

6.1.3 PELS with Type 4/4c IHS

Type 4/4c IHS = Type3/3c IHS + wider top side IHS

Figure 6.4 describes the PELS with top side IHS, naming Type 4 IHS and Type 4c IHS for OIO PELS module without and with top side cover, respectively, and Table 6-3 give suggested IHS size parameters.

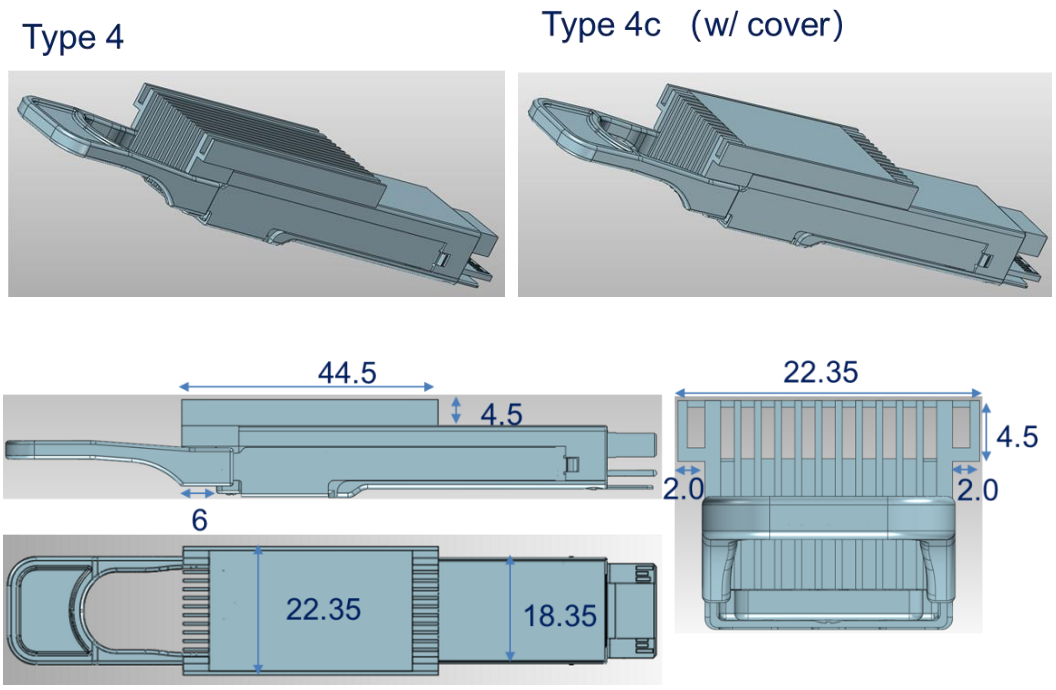


Figure 6.4 Type 4/4c IHS of OIO PELS

Table 6-3 Suggested size parameters of Type 4/4c IHS

IHS Size	**Parameters (mm)**	**Note**
Top IHS Height	4.5	
Side IHS Extended Width	2	Fins extend to two sides of PELS
Length	44.5	
Fin Total Width	22.35	
Fins Thickness	0.5	Suggested parameters, Could be adjusted with applications
Fin Pitch	1.5	
Fin Number	12	
Cover Size (Type 2A only)	≤38.5x22.35	

6.1.4 PELS with Type 5/5c IHS

Type 5/5c IHS = Type 4/4c IHS + extended Side IHS

Figure 6.5 describes the PELS with top side IHS, naming Type 5 IHS and Type 5c IHS for OIO PELS module without and with top side cover, respectively, and Table 6-4 give suggested IHS size parameters.

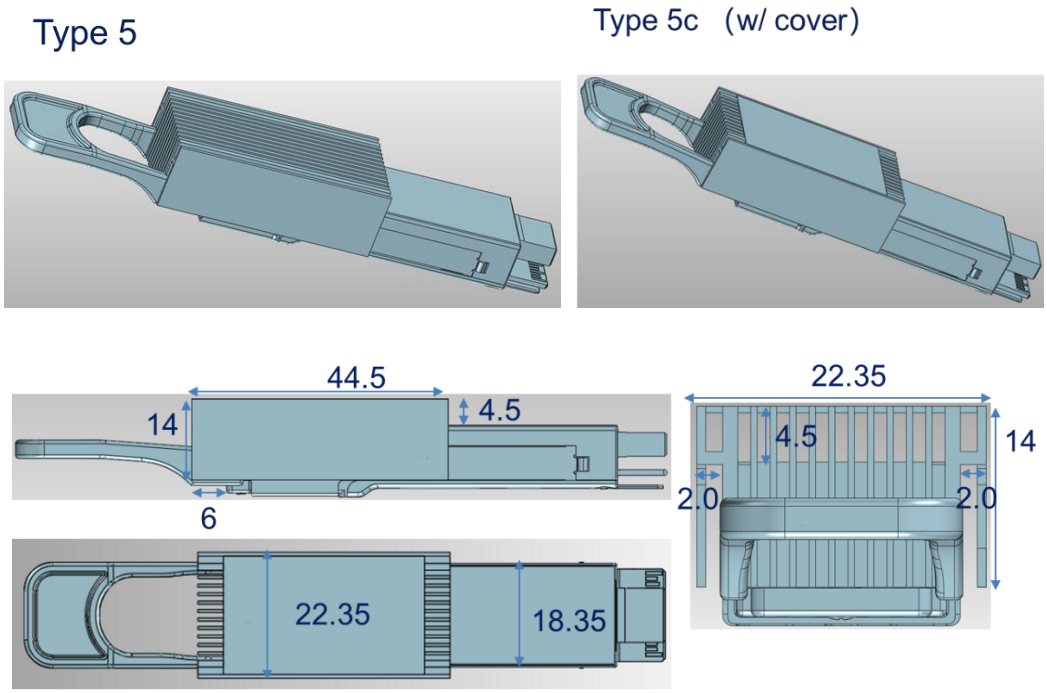


Figure 6.5 Type 5/5c IHS of OIO PELS

Table 6-4 Suggested size parameters of Type 5/5c IHS

IHS Size	**Parameters (mm)**	**Note**
Top IHS Height	4.5	
Aligned Side IHS Height	14	Side Fins extend to bottom shell of PELS; Suggested parameters, could be adjusted with applications
Side IHS Extended Width	2	Fins extend to two sides of PELS
Length	44.5	
Fin Total Width	22.35	
Fins Thickness	0.5	Suggested parameters, Could be adjusted with applications
Fin Pitch	1.5	
Fin Number	12	
Cover Size (Type 2A only)	≤38.5x22.35	

6.2 Label and Color Code

Each OIO PELS shall be clearly labeled with designated text as follows:

aa-#bb-cc-dd-ee

- ***aa***: MT ferrule types, MT12, MT16,etc.
- ***#***: number of fibers
- ***bb***: fiber types, single mode fiber (SMF) or polarization maintaining fiber (PMF)

- ***cc***: optical port mapping types, DR1, DR2 and FR for DR Type1, DR Type2 and FR Type, respectively, etc.
- ***dd***: optical power class in dBm
- ***ee***: heatsink types, IHS1, IHS2 and IHS2C for Type 1 IHS, Type 2 IHS and Type 2C IHS, respectively, etc.

Example Designations:

MT12-8PMF-DR1-19dBm-IHS2C

This OIO PELS has a MT12 ferrule with 8 PMFs supply single wavelength around 1311nm, and the population of the fibers follows the DR type1 as listed in Section 3.1, while the optical power supplied per fiber is at least 19dBm, and the integrated heatsink type is Type 2C IHS as listed in Section 6.1.1.

MT12-12PMF-FR-19dBm-IHS4

This OIO PELS has a MT12 ferrule with 12 PMFs supply single wavelength around 1311nm, and the population of the fibers follows the FR type as listed in Section 3.1, while the optical power supplied per fiber is at least 19dBm, and the integrated heatsink type is Type 4 IHS as listed in Section 6.1.3.

For the pull tab of the OIO PELS, it shall be in the color of **Yellow** so as to be clearly seen and to warn the operators of the laser security of OIO PELS.

7 Environmental Specifications

7.1 Temperature Class

Class	Module Case Temperature
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

7.2 Dust Proof

7.2.1 Module Side

A dust cap is needed to protect MT optical connector from dust and accident force after the PELS module assemble completed and module transport, as described in Figure 7.1.

Unused channel of the MT ferrule must be populated with dummy fiber to prevent dust contamination.

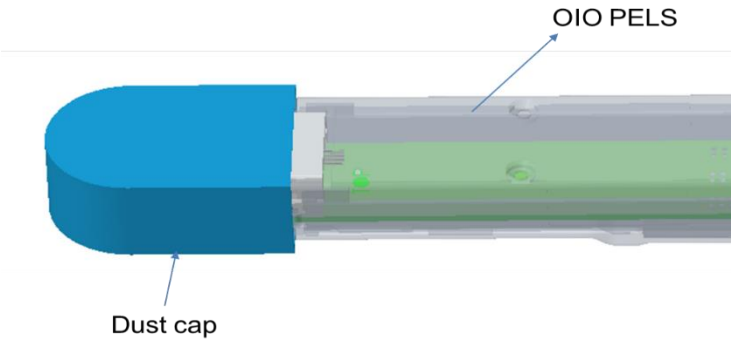


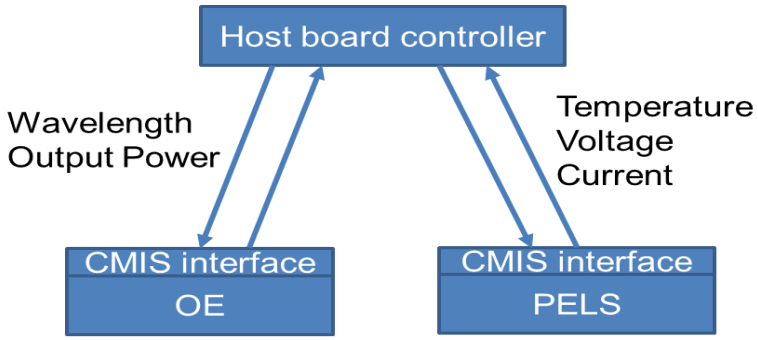
Figure 7.1 Dust cap for OIO PELS

7.2.2 Host side

As described in Figure 5.2, E/O hybrid connector contains a dust resist door to prevent dust contamination of host-side fibers.

8 PELS Common Management Interface Specification

The management interface for the PELS module are defined in the followings. The host communicates with PELS and OE over two-wire interface (TWI), includes the read/write operations to exchange temperature, voltage, current, lane output power, and wavelength information with the PELS and OE.



8.1 Timing Specifications

8.1.1 Introduction

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccLD, VccRx, Vcc_host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc_host on each of the TWI SCL (clock), SDA (data), and all low-speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

The PELS low speed electrical specifications are given in Table 8-1. This specification ensures compatibility between host bus masters and the TWI.

Table 8-1 Low speed control and sense signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA for fast mode, 20mA for Fast-mode plus
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms Pull up resistor, max
			200	pF	1.6 k Ohms Pull up resistor, max
LPMode/LDDis, Reset and ModeSelL	VIL	-0.3	0.8	V	| Iin | </= 125 uA for 0V < Vin < Vcc
	VIH	2	VCC+0.3	V	
IntL/RxLOS	VOL	0	0.4	V	IoL= 2.0 mA
	VOH	VCC-0.5	VCC+0.3	V	10 k ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IoL= 2.0 mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

8.1.2 Management Interface Timing Specification

The timing parameters for the TWI to the PELS module memory transaction timings are shown in Figure 8.1 and specified in Table 8-1 and is compatible with I2C. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. This clause closely follows the QSFP+ SFF-8636 specification but with the addition of Fast Mode+. This specification also defines tBUF timing, tWR timing, tNACK timing, tBPC timing.

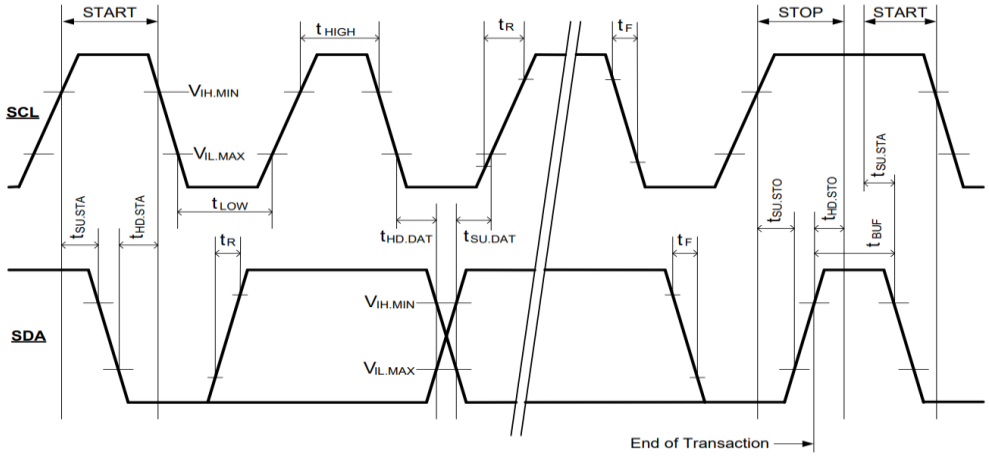


Figure 8.1 TWI Timing diagram

The TWI serial interface address of the PELS module is 1010000X (A0h). In order to allow access to multiple PELS modules on the same TWI serial bus, the PELS pinout includes a ModSelL or module select pin. This pin (which is pulled high, deselected in the module) must be held low by the host to select the module of interest and allow communication over the TWI serial interface. The module must not respond to or accept TWI serial bus instructions unless it is selected.

8.1.3 Serial Interface Protocol

The module asserts LOW for clock stretch on SCL.

8.1.3.1 Management Timing Parameters

The timing parameters for the TWI to the PELS module are shown in Table 8-2.

Table 8-2 Management interface timing parameters

TWI Modes		Fast Mode (400 kHz)		Fast Mode+ (1MHz)			
Module	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	kHz	
Clock Pulse Width Low	tLOW	1.3		0.5		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		20		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SCL starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	tR		300		120	ns	From (VL,MAX=0.3*Vcc) to (VIH,MIN=0.7*Vcc)
Input Fall Time	tF		300		120	ns	From (VIH,MIN=0.3*Vcc) to (VIL,MAX-=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		µs	
Aborted sequence-bus release	Deselect_Abort		2		2	ms	Delay from a host de-asserting ModSelL (at any

							point in a bus sequence) to the PELS module releasing SCL and SDA
ModSelL Setup Time	tSU.ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated TWI serial bus sequence
ModSelL Hold Time	tHD.ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a TWI serial bus sequence to changes of module select status
Seral Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500		500	μs	Time the PELS module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write to non-volatile Registers	tWR		80		80	ms	Time to complete a Single or Sequential Write to non-volatile registers
Accept a single or sequential write to volatile memory	tNACK		10		10	ms	Time to complete a Single or Sequential Write to volatile registers
Time to complete a memory bank/page	tBPC		10		10	ms	Time to complete a memory bank and/or page change
Endurance (Write Cycles)		50k		50k		cycles	Module Case Temperature = 70°C

8.2 Timing for Soft Control and Status Functions

Timing for PELS soft control and status functions are described in Table 8-3.

Table 8-3 I/O Timing for soft control and status functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInit Duration	Max MgmtInit Duration		2000	ms	Time from power on, hot plug or rising edge of reset until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.

ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
LPMode/LDDis mode change time	t_LPMode/LDDis		100	ms	Time to change between LPMode and LDDis modes of LPMode/LDDis
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, LD Fault and other flag bits.
LD Disable Assert Time	ton_LDDis		100	ms	Time from LD Disable bit set to 1 until optical output falls below 10% of nominal.
LD Disable Assert Time (optional fast mode)	ton_f_LDDis		3	ms	Optional fast mode is advertised via CMIS. Time from LDDis signal high to the optical output reaching the disabled level
LD Disable Deassert Time	toff_LDDis		400	ms	Time from LD Disable bit cleared to 1 until optical output rises above 90% of nominal.
LD Fault Assert Time	ton_LDfault		200	ms	Time from LD Fault state to LD Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b) until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b) until associated IntL operation resumes
Data Path LD Turn On Max Duration	DataPathLDTurnOn_MaxDuration				see CMIS memory P01h: B168

Data Path LD Turn Off Max Duration	DataPathLDTurnOff_MaxDuration	see CMIS memory P01h: B168
Data Path Deinit Max Duration	DataPathDeinit_MaxDuration	see CMIS memory P01h: B144
Data Path Init Max Duration	DataPathInit_MaxDuration	see CMIS memory P01h: B144
Module Pwr Up Max Duration	ModulePwrUp_MaxDuration	see CMIS memory P01h: B167
Module Pwr Dn Max Duration	ModulePwrDn_MaxDuration	see CMIS memory P01h: B167

8.3 State Machine

The following diagram in Figure 8.2 describes the state machine of PESL. Compared to CMIS 3.0, an Output Check Mode status is added to check whether the fiber links between the PELS and the OE module are contaminated or not, improving the reliability of OIO system.

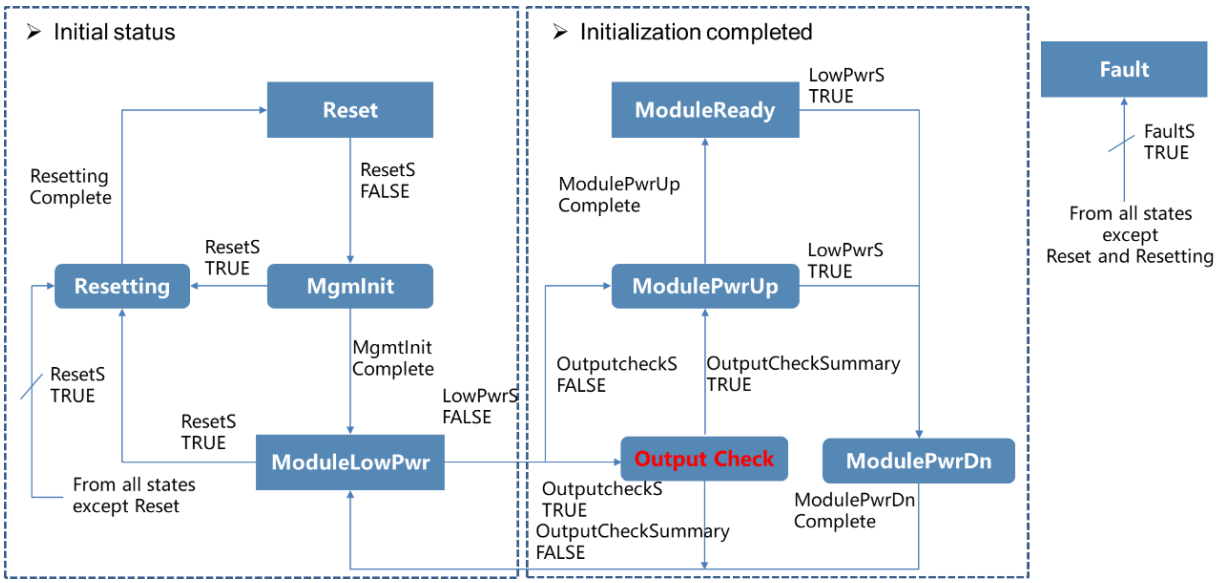


Figure 8.2 PELS initialization state machine flow

8.4 Read/Write Functionality

8.4.4 PELS Memory Address Counter (Read AND Write Operations)

PELS devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the module. This address stays valid between operations as long as PELS power is maintained. The address “roll over” during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

8.4.5 Read Operations (Current Address Read)

A current address read operation requires only the device address read word (101000001) be sent, see Table 8-4. Once acknowledged by the PELS, the current address data word is serially clocked out. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

Table 8-4 PELS Current address read operation

		←--PELS ADDR--→																		
HOST	START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
PELS										ACK	MSB							LSB		
											←--DATA WORD--→									

8.4.6 Read Operations (Random Read)

A random read operation requires a “dummy” write operation to load in the target byte address as shown in Table 8-5. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the PELS. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The PELS acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

Table 8-5 PELS Random read operation

		←--PELS ADDR--→									←--MEMORY ADDR--→										←--PELS ADDR--→																										
HOST	START	MSB						LSB	WRITE		MSB								LSB		START	MSB						LSB	READ															NACK	STOP	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1										
PELS										ACK									ACK									ACK	MSB								LSB										
																													←--DATA WORD--→																				

8.4.7 Read Operations (Sequential Read)

Sequential reads are initiated by either a current address read (Table 8-6) or a random address read (Table 8-7). To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the PELS receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

Table 8-6 Sequential address read starting at PELS current address

		←--PELS ADDR--→																																				
HOST	START	MSB						LSB	READ										ACK									ACK									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
PELS										ACK	MSB							LSB		MSB							LSB		MSB							LSB		
											←--DATA WORD n--→									←--DATA WORD n+1--→									←--DATA WORD n+x--→									

Table 8-7 Sequential address read starting with random PELS read

		←PELS ADDR→									←MEMORY ADDR→										←PELS ADDR→																																				
HOST	START	MSB						LSB	WRITE		MSB							LSB		START	MSB						LSB	READ										ACK									ACK									NACK	STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
PELS										ACK									ACK										ACK	MSB							LSB		MSB							LSB		MSB							LSB		
																														←DATA WORD n→									←DATA WORD n+1→									←DATA WORD n+x→									

8.4.8 Write Operations (BYTE Write)

A write operation requires an 8-bit data word address following the device address write word (10100000) and acknowledgement, see Table 8-8. Upon receipt of this address, the PELS shall again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the PELS shall output a zero (ACK) and the host master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the TWI specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the PELS enters an internally timed write cycle, tWR, to internal memory. The PELS disables it is management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that TWI “Combined Format” using repeated START conditions is not supported on PELS write commands.

Table 8-8 PELS Write byte operation

		←PELS ADDR→									←MEMORY ADDR→									←DATA WORD→									
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
PELS										ACK									ACK									ACK	

8.4.9 Write Operations (Sequential Write)

PELS shall support up to a 4 sequential byte write without repeatedly sending PELS address and memory address information as shown in Table 8-9. A “sequential” write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the PELS acknowledges receipt of the first data word, the host can transmit up to three more data words. The PELS shall send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that TWI “combined format” using repeated START conditions is not supported on PELS write commands.

Table 8-9 PELS Sequential write operation

		←PELS ADDR→									←MEMORY ADDR→									←DATA WORD 1→									←DATA WORD 2→									←DATA WORD 3→									←DATA WORD 4→									
HOST	START	MSB							LSB	WRITE	MSB								LSB	MSB							LSB	MSB								LSB	MSB								LSB	MSB								LSB	STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
PELS										ACK									ACK									ACK									ACK									ACK									ACK	

8.4.10 Write Operations (Acknowledge Polling)

Once the PELS internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the PELS respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

8.5 Memory Map

PELS management interface, as already commonly used in other form factors like QSFP and SFP, is specified in order to enable flexible use of the module by the user. The memory map for PELS is adapted from “Common Management Interface Specification (CMIS 5.3)”.

The memory map tables contained within this section include columns for passive cables (PC), active cables (AC), active optical cables (AO) and separable modules (SM). Depending on the PELS type, some common memory map parameters are optional. In each column, one of three options is specified: required (R), optional (O) or conditional upon another parameter which is optional (C). Entries with a dash (-) indicate that whether the byte or bit is required is not relevant.

8.5.1 PELS Memory Map Page Overview

In PELS memory map, page 06h and page 1Ah are newly added and defined for "lane advertising" and "lane state and control", respectively, as shown in Figure 8.3. The page 06h are used for high power characteristics, while the page 1Ah is a banked page with 8 lanes in 1 bank, and used for laser lane status monitor and control.

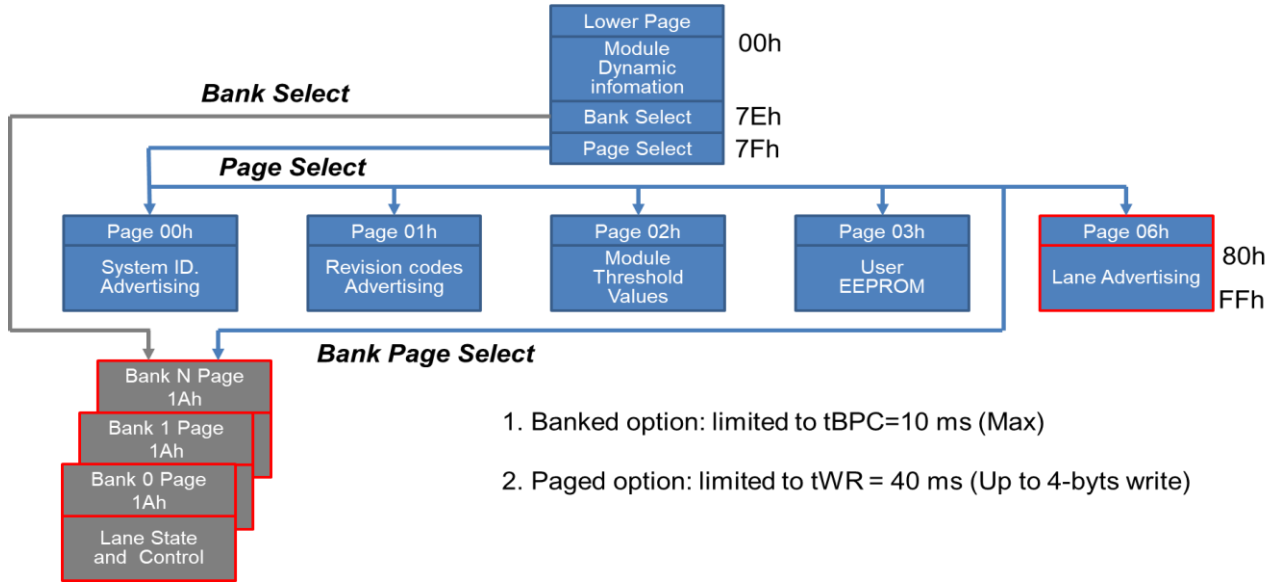
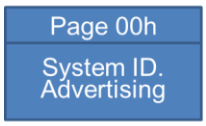
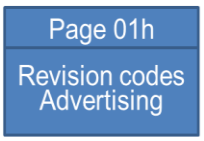


Figure 8.3 PELS memory map overview

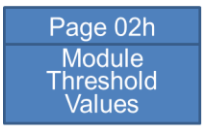
The corresponding memory map address in page 00h, page 01h and page 02h from CMIS 3.0 are modified as below:



Byte 0-2 Management Characteristics
Byte 3 and 26 Output check Mode
Byte 203 Connector Type
Reserved Byte 86-117 202 204-209 211



Byte 132-137 Supported PM Fiber
Byte 191 PELS Pages
Byte 145-160 Module Characteristics Advertising
Byte 161-162 Reserved



Byte 176-199 Move Power and Current Alarm Threshold to 06h

As for the memory map address in page 06h and page 1Ah, the register section are illustrated as Figure 8.4, and detail bytes definition are listed as Table 8-10 and Table 8-11.

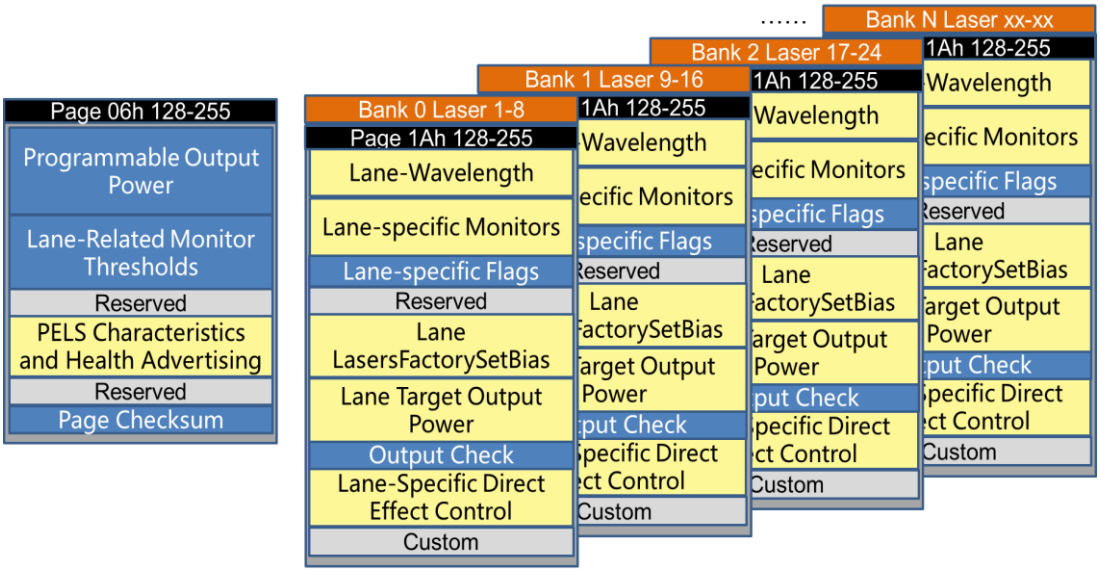


Figure 8.4 page 06h and page 1Ah register section definition

Table 8-10 Detail byte definitions of page 06h.

Byte	Size	Subject Area	Description	Type
128	1	Programmable Output Power Supported	Indicates Lane support for programmable output power.	RO
129-132	4	Programmable Output Power	Minimum and Maximum Programmable Output Power, 16-bit signed value in increment of 0.01 dBm.	RO
133-148	16	Lane-Related Monitor Thresholds	Threshold for Lane optical power and Lane bias	RO
149-150	2		Reserve	RW
151-160	10	PELS Characteristics Advertising		RO
161-180	20	PELS Health Advertising	PELS factory set parameters at room and high temperature	RO
161-220	40		Reserve	RW
221-254	34		Custom	RW
255	1	Page Checksum	Covers bytes 128-254	RO

Table 8-11 Detail byte definition of page 1Ah.

Byte	Size	Subject Area	Description	Type
128-143	16	Lane-Wavelength<n>	Output wavelength at room temperature, The laser wavelength value is equal to the 16-bit integer value of the wavelength in nm divided by 20 (units of 0.05 nm).	RO
144-175	32	Lane-specific Monitors	Generic media side monitors for optical power and laser bias	RO
176-184	9	Lane-specific Flags	Flags per lane	RO/ COR
185-192	8		Reserved	RW
193-208	16	LaneLasersFactorySetBias	Lasers Factory Set Bias for PELS Health Evaluation at room temperature and for high temperature	RW
209-224	16	LaneTargetOutputPower<n>	Target Output Power of lane<n>	RW
225	1	Output Check	The check flag for each output lane to confirm no dirty on the fiber output.	RW
226-235	10	Lane-Specific Direct Effect Control	Fields to control lane attributes control sets	RW
236-255	20		Custom	RW

In the following, the detail byte definitions are given.

Table 8-12 Detail byte definitions of traditional CMIS pages

Bytes	Size	Subject Area	Description	Type
2-Wire Serial Address 1010000x				
Lower Page 00h				
0-2	3	Management Characteristics	Basic Information about how this module is managed	RO
3	1	Global Status Information	Current state of Module, Interrupt signal status	RO
4-7	4	Flags Summary	Summary of Flags set on specific Pages (and Banks)	RO
8-13	6	Module-Level Flags	Flags that are not lane or Data Path specific	RO
14-25	12	Module-Level Monitors	Monitors that are not lane or Data Path specific	RO
26-30	5	Module-Level Controls	Controls applicable to the module as a whole	R/W
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags	R/W
37-38	2	CDB Command Status	Status of current CDB command	RO
39-40	2	Module Active Firmware Version	Module Active Firmware Version number	RO
41	1	Fault Information	Fault cause for entering ModuleFault state	RO
42-63	22		Reserved	R/W

64-84	21		Custom	R/W
85	1	MediaType	Media Type	RO
86-117	32		Reserved	R/W
118-125	8	Password Facilities	Password Entry and Change (mechanism only)	WO
126-127	2	Page Mapping	Page mapping into host addressable Upper Memory	R/W
Upper Page 00h				
128	1	SFF8024IdentifierCopy	Copy of Byte 00h: 0	RO
129-144	13	VendorName	Vendor name (ASCII)	RO
145-147	3	VendorOUI	Vendor IEEE company ID	RO
148-163	16	VendorPN	Part number provided by vendor (ASCII)	RO
164-165	2	VendorRev	Revision level for part number provided by vendor (ASCII)	RO
166-181	16	VendorSN	Vendor Serial Number (ASCII)	RO
182-189	8	DateCode	Manufacturing Date Code (ASCII)	RO
190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)	RO
200-201	2	ModulePowerCharacteristics	Module power characteristics	RO
202	1		Reserved	RO
203	1	ConnectorType	Connector type of the media interface	RO
204-209	6		Reserved	RO
210	1	MediaLaneInformation	Supported near end media lanes (all modules)	RO
211	1		Reserved	RO
212	1	MediaInterfaceTechnology	Information on media side device or cable technology	RO
213-220	8		Reserved	R/W
221	1		Custom	R/W
222	1	PageChecksum	Page Checksum over bytes 128-221	RO
223-255	33	Custom Information	Custom Information (non-volatile)	R/W
Page 01h (Optional)				
128-131	4	Inactive Firmware and Hardware revisions	Inactive FW revision and HW revision	RO
132-137	6	Supported link length	Supported lengths of various fiber media	RO
138-141	4	Wavelength Information	(for single wavelength modules)	RO
142	1	Supported Pages		RO
143-144	2	Durations Advertisements		RO
145-154	10	Module Characteristics		RO

155-156	2	Supported Controls		RO
157-158	2	Supported Flags		RO
159-160	2	Supported Monitors		RO
161-162	2	Supported Signal Integrity Controls		RO
162-166	4	Supported CDB Functionality		RO
167-169	3	Additional Durations Advertisements		RO
170-175	7		Reserved	RO
176-190	15	Media Lane advertising		RO
191-222	32		Custom	RO
223-250	28	Additional Application Descriptors		RO
251-254	4		Reserved	RO
255	1	Page Checksum	Page Checksum of bytes 130-254	RO
Page 02h (Optional)				
128-175	48	Module-level monitor thresholds		RO
176-199	24	Lane-specific monitor thresholds		RO
200-229	30		Reserved	RO
230-254	25		Custom	RO
255	1	Page Checksum	Covers bytes 128-254	RO
Page 03h (Optional)				
128-255	128	User Data	Module user data stored in NV memory	RO
Page 20h-7Fh (Optional)				
128	255		Reserved	R/W
Page 80h-FFh (Optional)				
128	255	Vendor Specific		R/W

8.5.2 Lower Page 00h

Lower Page 00h is used to access a variety of measurement, diagnostic and control functions. In addition, a mechanism to select upper memory map pages is provided. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

8.5.2.1 Management Characteristics (Page 00h, Bytes 0-2)

The Management Characteristics fields described in Table 8-13 provide fundamental management characteristics of the module that allow hosts to verify if, and to determine how, they can operate and manage the module.

The Management Characteristics fields include an SFF-8024 module type identifier (this is a value defined in the Identifier Values table in [5]) which implicitly contains information about the management protocol and the management Memory Map offered by the module.

Note: Since the management protocol is not systematically encoded in the SFF 8024 identifiers, hosts will have to

test against a list of supported SFF 8024 module type identifiers.

The other fields indicating management characteristics like the CMIS version number, memory model (flat memory or paged memory), support for intervention-free reconfiguration, and management interface speed, can be interpreted once the module has been recognized as a CMIS compliant module.

Note: Modules may also be classified by their functional "module type", depending on the unique or main Application that they support. This kind of "module type" is not encoded in the SFF8024Identifier field, but can instead be derived from other advertisements.

Table 8-13 Management Characteristics

Byte	Bit	Name	Description
0	All	SFF8024Identifier	28h QSFP-DD like interface
1	All	CmisRevision	CMIS revision number (decimal): The upper nibble (bits 7-4) is the integer part (major number) The lower nibble (bits 3-0) is the decimal part (minor number)
2	7	Reserved	Indicator of the memory model of the module: 0b: Paged memory (Pages 00h-02h, 10h-11h supported) 1b: Flat memory (Page 00h supported only)
	6	SteppedConfigOnly	0b: Module supports intervention-free reconfiguration 1b: Module supports only step-by-step reconfiguration, where a host WRITE to ApplyDPInit is (technically) accepted in all states without causing DPSM state changes, and where ApplyImmediate is not supported (i.e. a WRITE to ApplyImmediate is ignored).
	5-4	Reserved	
	3-2	MciMaxSpeed	Indicates maximum supported clock speed of Management Communication Interface (MCI): 00b: Module supports up to 400 kHz 01b: Module supports up to 1 MHz 10b: Reserved 11b: Reserved
	1-0	Reserved	

8.5.2.2 Global Status Information

The fields described in Table 8-14 provide fundamental module status indicators.

Table 8-14 Global Status Information

Byte	Bit	Name	Description
3	7-4	Reserved	
	3-1	ModuleState	Current Module State (see Table 8-15 for encoding and section 8.5.2.2 for a description of the meaning of ModuleState) Notes: - Flat memory modules always report ModuleReady.

			- Not all states of the Module State Machine are observable.
	0	InterruptDeasserted	Status of Interrupt output signal 1b: Interrupt not asserted (default) 0b: Interrupt asserted

Table 8-15 Module State Encodings

Code	Module State	Description
000b	-	Reserved
001b	ModuleLowPwr	
010b	ModulePwrUp	
011b	ModuleReady	This is the only state reported by flat memory modules
100b	ModulePwrDn	
101b	ModuleFault	
110b	ModuleOutputcheck	This state is used to check the link status
111b	-	Reserved

8.5.2.3 Flags Summary

The Flags Summary bits listed in Table 8-16 indicate when any Flags are asserted on specific pages, for up to 4 Banks.

Note: To clear a summarized Flag, the Flag itself must be read from the relevant Page on the appropriate Bank.

Table 8-16 Lane-Level Flags Summary

Byte	Bit	Name	Description
4	7		Reserved
	6		Reserved
	5		Reserved
	4	FlagsSummaryBank0Page1Ah	1b: at least one Flag is set on Bank 0, Page 1Ah
	3	FlagsSummaryBank0Page2Ch	1b: at least one Flag is set on Bank 0, Page 2Ch
	2	FlagsSummaryBank0Page14h	1b: at least one Flag is set on Bank 0, Page 14h
	1	FlagsSummaryBank0Page12h	1b: at least one Flag is set on Bank 0, Page 12h
	0	FlagsSummaryBank0Page11h	1b: at least one Flag is set on Bank 0, Page 11h
5	7		Reserved
	6		Reserved
	5		Reserved
	4	FlagsSummaryBank1Page1Ah	1b: at least one Flag is set on Bank 0, Page 1Ah
	3	FlagsSummaryBank1Page2Ch	1b: at least one Flag is set on Bank 1, Page 2Ch
	2	FlagsSummaryBank1Page14h	1b: at least one Flag is set on Bank 1, Page 14h
	1	FlagsSummaryBank1Page12h	1b: at least one Flag is set on Bank 1, Page 12h
	0	FlagsSummaryBank1Page11h	1b: at least one Flag is set on Bank 1, Page 11h
6	7		Reserved
	6		Reserved

	5		Reserved
	4	FlagsSummaryBank2Page1Ah	1b: at least one Flag is set on Bank 2, Page 1Ah
	3	FlagsSummaryBank2Page2Ch	1b: at least one Flag is set on Bank 2, Page 2Ch
	2	FlagsSummaryBank2Page14h	1b: at least one Flag is set on Bank 2, Page 14h
	1	FlagsSummaryBank2Page12h	1b: at least one Flag is set on Bank 2, Page 12h
	0	FlagsSummaryBank2Page11h	1b: at least one Flag is set on Bank 2, Page 11h
7	7		Reserved
	6		Reserved
	5		Reserved
	4	FlagsSummaryBank3Page1Ah	1b: at least one Flag is set on Bank 3, Page 1Ah
	3	FlagsSummaryBank3Page2Ch	1b: at least one Flag is set on Bank 3, Page 2Ch
	2	FlagsSummaryBank3Page14h	1b: at least one Flag is set on Bank 3, Page 14h
	1	FlagsSummaryBank3Page12h	1b: at least one Flag is set on Bank 3, Page 12h
	0	FlagsSummaryBank3Page11h	1b: at least one Flag is set on Bank 3, Page 11h

8.5.2.4 Module-Level Flags

The registers described in Table 8-17 contain module-level (global) Flags, with Masks described in Section 8.5.2.7.

Module-level Flags are used to report module-level status changes, operating failures, as well as threshold crossing alarms and warnings for monitored observables. Monitors with associated alarm and/or warning thresholds have associated alarm Flags, warning Flags. For normal operation and in default state, these Flags are cleared.

Byte 13 is provided for Custom Module Level Flags.

Table 8-17 Module Flags (paged memory modules only)

Byte	Bit	Name	Description
8	7	CdbCmdCompleteFlag2	Latched Flag to indicate completion of a CDB command for CDB instance 2. Support is advertised in field 01h:163.7-6
	6	CdbCmdCompleteFlag1	Latched Flag to indicate completion of a CDB command for CDB instance 1. Support is advertised in field 01h:163.7-6
	5-3		Reserved
	2		Reserved
	1	ModuleFirmwareErrorFlag	Latched Flag to indicate that self-supervision of the main module firmware has detected a failure in the main module firmware itself. There are several possible causes of the error such as program memory becoming corrupted and incomplete firmware loading.
	0	ModuleStateChangedFlag	Latched Flag to indicate a Module State Change
9	7	VccMonLowWarningFlag	Latched Flag for low supply voltage warning
	6	VccMonHighWarningFlag	Latched Flag for high supply voltage warning
	5	VccMonLowAlarmFlag	Latched Flag for low supply voltage alarm

	4	VccMonHighAlarmFlag	Latched Flag for high supply voltage alarm
	3	TempMonLowWarningFlag	Latched Flag for low temperature warning
	2	TempMonHighWarningFlag	Latched Flag for high temperature warning
	1	TempMonLowAlarmFlag	Latched Flag for low temperature alarm
	0	TempMonHighAlarmFlag	Latched Flag for high temperature alarm
10	7	Aux2MonLowWarningFlag	Latched Flag for low Aux 2 monitor warning
	6	Aux2MonHighWarningFlag	Latched Flag for high Aux 2 monitor warning
	5	Aux2MonLowAlarmFlag	Latched Flag for low Aux 2 monitor alarm
	4	Aux2MonHighAlarmFlag	Latched Flag for high Aux 2 monitor alarm
	3	Aux1MonLowWarningFlag	Latched Flag for low Aux 1 monitor warning
	2	Aux1MonHighWarningFlag	Latched Flag for high Aux 1 monitor warning
	1	Aux1MonLowAlarmFlag	Latched Flag for low Aux 1 monitor alarm
	0	Aux1MonHighAlarmFlag	Latched Flag for high Aux 1 monitor alarm
11	7	CustomMonLowWarningFlag	Latched Flag for low Vendor Defined Monitor warning
	6	CustomMonHighWarningFlag	Latched Flag for high Vendor Defined Monitor warning
	5	CustomMonLowAlarmFlag	Latched Flag for low Vendor Defined Monitor alarm
	4	CustomMonHighAlarmFlag	Latched Flag for high Vendor Defined Monitor alarm
	3	Aux3MonLowWarningFlag	Latched Flag for low Aux 3 monitor warning
	2	Aux3MonHighWarningFlag	Latched Flag for high Aux 3 monitor warning
	1	Aux3MonLowAlarmFlag	Latched Flag for low Aux 3 monitor alarm
	0	Aux3MonHighAlarmFlag	Latched Flag for high Aux 3 monitor alarm
12	All		Reserved
13	All		Custom

8.5.2.5 Module-Level Monitor Values

Real time monitoring for module-level observables includes two monitors with fixed observables (temperature and supply voltage) and four monitors with selectable function (3 auxiliary and 1 vendor defined) as shown in Table 8-18.

Note: The data format of a monitored value may have greater resolution and range than required.

Measurement accuracy is defined by the relevant interface standard or module product specification.

The reported monitoring results of supported module level monitors shall be within the relevant accuracy requirements when the module is in the ModuleReady state.

Table 8-18 Module-Level Monitor Values (paged memory modules only)

Byte	Bit	Name	Description
14-15	All	TempMonValue	S16 Module Temperature Monitor (Current Value) internally measured temperature in 1/256 degree Celsius increments
16-17	All	VccMonVoltage	U16 Supply Voltage Monitor (Current Value) internally measured input supply voltage in 100 µV increments
18-19	All	Aux1MonValue	S16 Aux1 Monitor (see Table 8-44) (Current Value)

			The monitored observable is advertised in 01h:145.0: 0b: Custom 1b: TEC Current in 100%/32767 increments of maximum TEC current magnitude, i.e. of the larger of the heating or cooling current magnitudes +32767 (100%) of the max current magnitude when heating -32767 is -100% of the max current magnitude when cooling
20-21	All	Aux2MonValue	S16 Aux2 Monitor (see Table 8-44) (Current Value) The monitored observable is advertised in 01h:145.1: 0b: Laser Temperature: in 1/256 degree Celsius increments 1b: TEC Current in 100%/32767 increments of maximum TEC current magnitude, i.e. of the larger of the heating or cooling current magnitudes +32767 (100%) of the max current magnitude when heating -32767 is -100% of the max current magnitude when cooling
22-23	All	Aux3MonValue	S16 Aux3 Monitor (see Table 8-44) (Current Value) The monitored observable is advertised in 01h:145.2: 0b: Laser Temperature: in 1/256 degree Celsius increments 1b: Additional Supply Voltage: in 100 µV increments
24-25	All	CustomMonValue	S16 or U16: Custom monitor (Current Value)

8.5.2.6 Module-Level Controls

Module-Level (global) controls, as listed in Table 8-19 are applicable to the entire module or to all Lanes or Data Paths in the module.

Note: Lane-specific controls are located in Page 1Ah (see Section 8.5.9).

Table 8-19 Module Global Controls (paged memory modules only)

Byte	Bit	Name	Description
26	7	BankBroadcastEnable	0 b: Bank broadcast for lane-banked pages disabled 1b: Bank broadcast for lane-banked pages enabled When BankBroadcastEnable is set, a WRITE to a control register (i.e. to a register with RW or WO access) in any bank of a lane-banked page is executed as a bank broadcast. Recall that a banked page is lane-banked if banking is used to add support for additional lanes. A bank broadcast is a virtually simultaneous and atomic WRITE of the same value to the same register and the same page, in all supported banks. The module ensures a generalized broadcast register readback condition, such that a READ from any supported bank for the same page and register always yields the value written in the broadcasted WRITE. Advertisement: 01h:156.7

	6	LowPwrAllowRequestHW	Enables evaluation of the LowPwrRequestHW hardware signal 0b: Module ignores the LowPwrRequestHW signal 1b: Module evaluates the LowPwrRequestHW signal (default) Note: See Figure 8.2 and Section 8.3 for more information Note: As LowPwrRequestSW is cleared by default, evaluation of LowPwrRequestHW is enabled by default, allowing the host to request start-up to halt in Low Power mode.
	5	OutputcheckAllowRequestSW	Enables evaluation of the OutputcheckAllowRequestSW hardware signal 0b: Module ignores the OutputcheckAllowRequestSW signal 1b: Module evaluates the OutputcheckAllowRequestSW signal (default)
	4	LowPwrRequestSW	0b: No request 1b: Request for the module to stay in, or to return into, Low Power mode
	3	SoftwareReset	Self-clearing trigger bit that causes the module to be reset when 1b is written to it. The effect of a SoftwareReset trigger is the same as asserting the Reset hardware signal for the appropriate hold time, followed by its de-assertion. 0b: No action 1b: Software reset
	2-0		Custom
27-28	All		Reserved
29-30	All		Custom

8.5.2.7 Module-Level Masks

The host can control which Flags may cause a hardware Interrupt by setting Mask bits described in Table 8-20.

Table 8-20 Module Level Masks (paged memory modules only)

Byte	Bit	Name	Description
31	7	CdbCmdCompleteMask2	Mask bit for CdbCmdCompleteFlag2
	6	CdbCmdCompleteMask1	Mask bit for CdbCmdCompleteFlag1
	5-2		Reserved
	1	ModuleFirmwareErrorMask	Mask bit for ModuleFirmwareErrorFlag
	0	ModuleStateChangedMask	Mask bit for ModuleStateChangedFlag
32	7	VccMonLowWarningMask	Mask bit for VccMonLowWarningFlag
	6	VccMonHighWarningMask	Mask bit for VccMonHighWarningFlag

	5	VccMonLowAlarmMask	Mask bit for VccMonLowAlarmFlag
	4	VccMonHighAlarmMask	Mask bit for VccMonHighAlarmFlag
	3	TempMonLowWarningMask	Mask bit for TempMonLowWarningFlag
	2	TempMonHighWarningMask	Mask bit for TempMonHighWarningFlag
	1	TempMonLowAlarmMask	Mask bit for TempMonLowAlarmFlag
	0	TempMonHighAlarmMask	Mask bit for TempMonHighAlarmFlag
33	7	Aux2MonLowWarningMask	Mask bit for Aux2MonLowWarningFlag
	6	Aux2MonHighWarningMask	Mask bit for Aux2MonHighWarningFlag
	5	Aux2MonLowAlarmMask	Mask bit for Aux2MonLowAlarmFlag
	4	Aux2MonHighAlarmMask	Mask bit for Aux2MonHighAlarmFlag
	3	Aux1MonLowWarningMask	Mask bit for Aux1MonLowWarningFlag
	2	Aux1MonHighWarningMask	Mask bit for Aux1MonHighWarningFlag
	1	Aux1MonLowAlarmMask	Mask bit for Aux1MonLowAlarmFlag
	0	Aux1MonHighAlarmMask	Mask bit for Aux1MonHighAlarmFlag
34	7	CustomMonLowWarningMask	Mask bit for CustomMonLowWarningFlag
	6	CustomMonHighWarningMask	Mask bit for CustomMonHighWarningFlag
	5	CustomMonLowAlarmMask	Mask bit for CustomMonLowAlarmFlag
	4	CustomMonHighAlarmMask	Mask bit for CustomMonHighAlarmFlag
	3	Aux3MonLowWarningMask	Mask bit for Aux3MonLowWarningFlag
	2	Aux3MonHighWarningMask	Mask bit for Aux3MonHighWarningFlag
	1	Aux3MonLowAlarmMask	Mask bit for Aux3MonLowAlarmFlag
	0	Aux3MonHighAlarmMask	Mask bit for Aux3MonHighAlarmFlag
35	All		Reserved for Masks
36	All		Custom Module level Masks

8.5.2.8 CDB Command Status

The CDB command status fields CdbStatus<i> provide the status of the most recently triggered CDB command execution or its result, separately for each CDB Instance <i>.

When CDB is used in background operation mode (see Table 8-21, the host can read the relevant CDB command status field while a CDB command is executing to obtain its current status.

When CDB is used in foreground operation mode, the host can read the relevant CDB command status field only after the command has completed, as can be determined by Acknowledge polling.

Table 8-21 CdbStatus fields (paged memory modules only)

Byte	Bit	Name	Description
37	All	CdbStatus1	Status of the most recent CDB command in CDB instance 1
38	All	CdbStatus2	Status of the most recent CDB command in CDB instance 2

A CdbStatus field has the following format in Table 8-22:

Table 8-22 Bit definitions within CdbStatus fields

Bits	Field Name	Field Description
7	CdbIsBusy	Bool: CdbIsBusy status bit indicates whether the module is still busy, or idle and ready to accept a new CDB command 0b: Module idle, host can write 1b: Module busy, host needs to wait
6	CdbHasFailed	Bool: CdbHasFailed bit indicates if there was a failure, after the module has completed execution of the last CDB command 0b: Last triggered CDB command completed successfully 1b: Last triggered CDB command failed
5-0	CdbCommandResult	The CdbCommandResult field provides more detail classification for each of the three coarse query results that are encoded by the pair of bit 7 (CdbIsBusy) and bit 6 (CdbHasFailed) Coarse Status CdbIsBusy CdbHasFailed IN PROGRESS 1 X (don't care) SUCCESS 0 0 FAILED: 0 1 The interpretation of CdbCommandResult therefore depends on the coarse status as follows: IN PROGRESS 00h=Reserved 01h=Command is captured but not processed 02h=Command checking is in progress 03h=Command execution is in progress 04h-2Fh=Reserved 30h-3Fh=Custom SUCCESS 00h=Reserved 01h=Command completed successfully 02h=Reserved 03h=Previous CMD was ABORTED by CMD Abort 04h-1Fh=Reserved 20h-2Fh=Reserved 30h-3Fh=Custom FAILED 00h=Reserved 01h=CMDID unknown 02h=Parameter range error or parameter not supported 03h=Previous CMD was not properly ABORTED (by CMD Abort) 04h=Command checking time out 05h=CdbChkCode Error 06h=Password related error (command specific meaning) 07h=Command not compatible with operating status 08h-0Fh=Reserved for STS command checking error 10h-1Fh=Reserved 20h-2Fh=For individual STS command or task error 30h-3Fh=Custom

The module sets the CdbIsBusy bit when a CDB command is triggered on the respective CDB instance.

The module clears the CdbIsBusy bit on successful or unsuccessful completion of a CDB command, after updating the fields describing the result of the completed command

- The CdbHasFailed bit reports if the command has failed
- The CdbCommandResult field provides a detail classification

After command completion, the module does not change the CdbStatus byte of a CDB Instance, until the next CDB command is triggered for that CDB instance.

8.5.2.9 Module Active Firmware Version

The Bytes described in Table 8-23 allow a module to report the firmware major and minor revision for the active (i.e. currently running) firmware, or to indicate that no firmware is running.

Note: Module firmware may consist of multiple firmware components (program images, non-volatile data). It is strongly recommended that the firmware version identifies the aggregate (or bundle) of all firmware elements that can be updated by the vendor or by the host.

Note: For modules supporting firmware update, it is also strongly recommended that the firmware major and minor revision numbers together with build number (available by CDB query) uniquely specifies exactly one aggregate firmware configuration. Firmware aggregates that differ in only a single component should never have the same version identification (major, minor, build).

Note: The identification of temporary firmware component versions for lab test or debug, or identification of individual firmware components is not in the scope of this specification. However, the CDB firmware query command supports additional fields which could be used to mark such temporary firmware aggregates.

Reporting firmware version information is generally required and independent of whether a module supports firmware update by any method.

Content and meaning of firmware major and minor revision information reported are vendor dependent, but the format of both fields is defined to be integer. The encoding of the major and minor revision fields is:

- Major Revision = 0 and Minor Revision = 0 indicates that a module does not have any firmware.
- Major Revision = FFh and Minor Revision = FFh indicates that the active firmware image is invalid1.
- All other Major and Minor Revision combinations indicate the active firmware version.

Table 8-23 Module Active Firmware Version

Byte	Bit	Name	Description
39	All	ModuleActiveFirmwareMajorRevision	U8 Numeric representation of the module's active firmware major revision
40	All	ModuleActiveFirmwareMinorRevision	U8 Numeric representation of the module's active firmware minor revision

8.5.2.10 Module Fault Information

The optional ModuleFaultCause Byte in Table 8-24 describes the reason for the module having entered the ModuleFault state.

Table 8-24 Fault Information (paged memory modules only)

Byte	Bit	Name	Description
41	All	ModuleFaultCause	Reason of entering the ModuleFault state 0: No Fault detected (or field not supported) 1: TEC runaway 2: Data memory corrupted 3: Program memory corrupted 4-31: Reserved (fault codes) 32-63: Custom (fault codes) 64-255: Reserved (general)

8.5.2.11 Applications Advertising

Bytes 00h: 86-117 (see Table 8-25) provide space for an array of the first four of five bytes (see Table 8-24) of eight Application Descriptors.

All parts of the Application Descriptor are linked by a number known as the AppSel Code, which is simply the sequential position number of the Application Descriptor in any of the memory locations storing (parts of) the Application Descriptor array.

Table 8-25 Media Type Encodings

Code	Media Type	Associated Interface ID Table
00h	Undefined	None, not applicable
01h	Optical Interfaces: MMF	“850 nm MM media interface codes”
02h	Optical Interfaces: SMF	“SM media interface codes”
03h	Passive Copper Cables	“Passive Copper Cable interface codes”
04h	Active Cables	“Active Cable assembly interface codes”
05h	BASE-T	“BASE-T media interface codes”
06h	Optical Interfaces: PMF	“1310 nm PM media interface codes”
07h-3Fh		Reserved
40h-8Fh		Custom
90h-FFh		Reserved

Table 8-26 Media Type Register (Lower Memory)

Byte	Bit	Name	Description
85	All	MediaType	The MediaType field defines the interpretation values in the following Application Descriptors. See Table 8-25 for the MediaType encoding.

8.5.2.12 Password Entry and Change

The password entry and change facility described in this section provides a standardized mechanism to allow password protection of custom data or functionality, which itself are outside of the scope of this specification.

Note: An alternative password entry and password change mechanism providing feedback about success or failure is available via CDB commands CMD 0001h and CMD 0002h.

Password protected custom functionality and password entry mechanism support is optional (there is no advertisement) but if it is supported, it shall conform to the following specifications.

Password protection of CMIS specified data or functionality is prohibited for CMIS compliant module, unless explicitly specified1 or advertised2.

The password entry and change facility uses 32-bit passwords (U32 values in Big-Endian hex notation).

A password entry register must be written using a size-matched four-byte WRITE access

Password entry registers are self-clearing; the module maintains the state of password protection internally.

In the password value range, two types of passwords are distinguished:

A Host Password value is in the range of 0000 0000h to 7FFF FFFFh. It can be changed by the host.

A Module Password value is in the range of 80000000h to FFFF FFFFh. It cannot be changed by the host.

Note: A host password may e.g. be used to protect module instance-specific data (e.g. inventory data) that are under control of the module user. A module password may e.g. be used by module vendors to grant access to custom features only to those hosts who have been given a certain module password.

The factory default of a Host Password is 0000 1011h.

The factory default of a Module Password is defined by the module vendor.

The host can change a current Host Password value by writing a new Host Password value into the Password Change Entry Area (Bytes 118-121) after the correct current Host Password value has been entered into the Password Entry Area (Bytes 122-125). The effect of writing a Module Password value is undefined.

Password-protected features are unlocked when a valid password is entered and remain unlocked until either an invalid password is entered or until the module is reinitialized.

The initial internal state of password protection when the module exits the MgmtInit state shall be locked.

Table 8-27 Password Change Entry

Byte	Bit	Name	Description
118-121	All	PasswordChangeEntryArea	U32: new password value
122-125	All	PasswordEntryArea	U32: password value

8.5.2.13 Page Mapping (Upper Memory Content Selection)

The PageMapping register (00h:126-127, as listed in Table 8-28) is a two-byte register containing a Page Address value that determines which register in the internal Management Memory Map is actually accessed when the host performs an ACCESS addressing a Byte in Upper Memory (Byte address range 128-255).

Table 8-28 Page Mapping Register Components

Byte	Bit	Name	Description
126	All	BankSelect	Bank Index of Page mapped to Upper Memory (if applicable). The current BankSelect value determines which Bank of a Page is accessed (for Pages with Banking) when a host ACCESS addresses a Byte in Upper Memory (address 128 through 255). Ignored when the Page indexed by PageSelect is unbanked.
127	All	PageSelect	Page Index of Page mapped to Upper Memory The current PageSelect value determines which Page (or Page in a Bank) is accessed when a host ACCESS addresses a Byte in Upper Memory (address 128 through 255) Note: The module may clear the PageSelect to prevent mapping an unsupported page.

Note: This programmable redirection from a fixed Upper Memory address window to a selected Page in the Management Memory Map is referred to as Page Mapping. Note that CMIS is agnostic of how a module actually implements or emulates page mapping.

The PageMapping register has two components storing the two components of a Page Address:

- The BankSelect Byte (00h:126) storing a Bank Index
- The PageSelect Byte (00h:127) storing a Page Index

Note: Beware of confusion – a Page Address is a two-dimensional value that uniquely identifies a Page, whereas a Page Index is a one-dimensional value identifying a set of Pages with the same Bank Index.

The Management Memory Map defines banked Pages (with the potential of Bank Support) and unbanked Pages (without Bank Support), whereby the Bank Index of unbanked Pages is irrelevant (albeit using a nominal value of 0 is recommended).

Note: See Section 8.5.1 for background on the host accessible Management Memory Map, on the split of host addressable memory into LowerMemory and UpperMemory, and on Banking.

For an arbitrary Page Address change or for just a Bank Index change, a host must write both BankSelect and PageSelect in one WRITE access, even if the PageSelect value does not change. The module does not begin processing the BankSelect value until after the PageSelect register has been written.

For just a Page Index change (mapping another Page in the current Bank), or for mapping an arbitrary unbanked Page to Upper Memory, a host may WRITE only the PageSelect Byte.

PageMapping Validity

The module ensures that the PageMapping register always contains a Page Address that is actually supported by the module: When a host write would result in a not supported Page Address in the PageMapping register, the module clears the PageSelect Byte (without clearing the BankSelect Byte), such that the resulting PageMapping register selects Page 00h (as the BankSelect value is ignored unbanked Page 00h).

Note: This is a deliberate exception from the usual rule that either host or module modify a field, but not both.

Stale Data Access Prevention during Page Remapping

The module may need time to effectively switch the content of Upper Memory (i.e. to effectively map a new Page) after a change of the PageMapping register.

8.5.3 Page 00h (Administrative Information)

Page 00h contains static read-only module characteristic information.

Page 00h is supported by all modules (including cable assemblies).

Table 8-29 Page 00h Overview

Byte	Size	Name	Description
128	1	SFF8024IdentifierCopy	Copy of Byte 00h:0
129-144	16	VendorName	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vender Rev	Revision level for part number provided by vendor (ASCII)
1676-181	16	VendorSN	Vendor Serial Number (ASCII)
182-189	8	DateCode	Manufacturing Date Code (ASCII)
190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)
200-201	2	ModulePowerCharacteristics	Module power characteristics
202	1		Reserved
203	1	ConnectorType	Connector type of the media interface
204-209	6		Reserved
210	1	MediaLaneInformation	Supported near end media lanes (all modules)
211	1		Reserved
212	1	MediaInterfaceTechnology	Information on media side device or cable technology
213-220	8		Reserved
221	1		Custom
222	1	PageChecksum	Page Checksum over bytes 128-221
223-255	33		Custom Information (non-volatile)

8.5.3.1 SFF-8024 Identifier Copy

This field shall contain the same value as Byte 00h:0.

8.5.3.2 Vendor Information

Vendor Name

The VendorName is a 16 character read-only field that contains ASCII characters, left aligned and padded on the

right with ASCII spaces (20h).

The VendorName shall contain the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. The VendorName may be the original manufacturer of the module or the name of the module reseller. In both cases, the VendorName and VendorOUI (if specified) shall correlate to the same company. At least one of the VendorName or the VendorOUI fields shall contain valid serial number manufacturing data.

Vendor Organizationally Unique Identifier

The vendor organizationally unique identifier field (VendorOUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the vendor's OUI is unspecified.

Vendor Part Number

The vendor part number (VendorPN) is a 16-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor part number is unspecified.

Vendor Revision Number

The vendor revision number (VendorRev) is a 2-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the field indicates that the vendor revision number is unspecified.

Vendor Serial Number

The vendor serial number (VendorSN) is a 16-character field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the Product. A value of all zero in the 16-byte field indicates that the vendor serial number is unspecified.

Date Code

The DateCode is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the following format:

Table 8-30 Date Code (Page 00h)

Byte	Size	Name	Description
182-183	All	Year	ASCII two low order digits of year (00=2000)
184-185	All	Month	ASCII digits of month (01=Jan through 12=Dec)
186-187	All	DayofMonth	ASCII day of month (01-31)
188-189	All	LotCode	ASCII custom lot code, may be blank

CLEI Code

The CLEI (Common Language Equipment Identification) code is a 10-byte field that contains the vendor's CLEI code in ASCII characters.

The CLEI code value is optional. If CLEI code value is not supported, a value of all ASCII 20h (spaces) shall be entered.

Table 8-31 CLEI Code (Page 00h)

Byte	Size	Name	Description
190-199	All	CLEICode	Vendor's CLEI Code (ASCII)

8.5.3.3 Module Power Characteristics

Module power characteristics are advertised in Bytes 00h:200 and 00h:201 (see Table 8-32). Specific max power in corresponding power class can be find in Section 4.3.

The MaxPower field specifies worst case maximum power consumption over operating conditions and lifetime.

The ModulePowerClass field provides a form factor specific classification of the MaxPower value.

Table 8-32 Module Power Class and Max Power (Page 00h)

Byte	Size	Name	Description
200	7-4	ModulePowerClass	0000: Power class 1, 1.5W 0001: Power class 2, 3.5W 0010: Power class 3, 7.0W 0011: Power class 4, 8.0W 0100: Power class 5, 9.0W 0101: Power class 6, 12W 0110: Power class 7, 15W 0111: Power class 8, 18W 1000: Power class 9, 21W 1001: Power class 10, >21W, TBD 1010: Power class 11, >21W, TBD 1011: Power class 12, >21W, TBD 1100: Power class 13, >21W, TBD 1101: Power class 14, >21W, TBD 1110: Power class 15, >21W, TBD 1111: Power class 16, >21W, TBD
	3-0		Reserved
201	All	MaxPower	Maximum power consumption in multiples of 0.1 W rounded up to the next whole multiple of 0.1 W

8.5.3.4 Media Connector Type

The ConnectorType field indicates the connector type for the media side of the module, as defined and maintained in the Connector References section of SFF-8024.

Table 8-33 Media Connector Type (Page 00h)

Byte	Size	Name	Description
203	All	ConnectorType	Type of connector present in the module.

8.5.3.5 Media Lane Information

The MediaLaneUnsupported Byte (see Table 8-34) indicates which Media Lanes are not supported.

Table 8-34 Media Lane Information (Page 00h)

Byte	Size	Name	Description
210	7	MediaLaneUnsupportedLane8	Bool: MediaLaneUnsupportedLane<i> 0b: Media Lane <i> supported 1b: Media Lane <i> not supported Condition: Module supports at most 8 host lanes. Otherwise, byte is reserved (0 valued). Hosts should ignore this byte when the module supports more than 8 host lanes.
	6	MediaLaneUnsupportedLane7	
	5	MediaLaneUnsupportedLane6	
	4	MediaLaneUnsupportedLane5	
	3	MediaLaneUnsupportedLane4	
	2	MediaLaneUnsupportedLane3	
	1	MediaLaneUnsupportedLane2	
	0	MediaLaneUnsupportedLane1	

8.5.3.6 Media Interface Technology

The MediaInterfaceTechnology Byte 00h:212 classifies the media interface device or cable technology, using the encodings in Table 8-35.

An active optical cable may be distinguished from a separable module by examining the ConnectorType field Byte 00h:203 (see Section 8.5.3.4), with values defined in the Connector References section of SFF-8024.

Table 8-35 Media Connector Type (Page 00h)

Byte	Size	Name	Description
212	All	MediaInterfaceTechnology	Media Interface Technology as per Table 8-36

Table 8-36 Media Interface Technology encodings

Code	Description of physical device
00h	850 nm VCSEL
01h	1310 nm VCSEL
02h	1550 nm VCSEL
03h	1310 nm FP
04h	1310 nm DFB
05h	1550 nm DFB
06h	1310 nm EML
07h	1550 nm EML
08h	Others
09h	1490 nm DFB
0Ah	Copper cable unequalized
0Bh	Copper cable passive equalized

0Ch	Copper cable, near and far end limiting active equalizers
0Dh	Copper cable, far end limiting active equalizers
0Eh	Copper cable, near end limiting active equalizers
0Fh	Copper cable, linear active equalizers
10h	C-band tunable laser
11h	L-band tunable laser
12h-FFh	Reserved

8.5.3.7 Page 00h Page Checksum (required)

The page checksum is a one-byte code that can be used to verify that the read-only static data on Page 00h is valid. The page checksum value shall be the low order 8 bits of the arithmetic sum of all byte values from byte 128 to byte 221, inclusive.

8.5.3.8 Custom Info (non-volatile)

Bytes 223-255 are allocated in non-volatile storage for information provided by the original manufacturer of the module or the module reseller. This information persists across module reset and power cycle.

The contents of this area are not defined by this specification.

8.5.4 Page 01h (Advertising)

Page 01h is an optional Page containing advertising fields for properties of paged memory modules.

The module advertises support of Page 01h in the MemoryModel Bit 00h:2.7.

Note: Page 01h is mandatory for paged memory modules.

All fields on Page 01h are read-only and static.

See the following subsections for detail information on the subject areas listed in Table 8-37.

Table 8-37 Page 01h Overview

Byte	Size	Name	Description
128-131	4	Inactive Firmware and Hardware revisions	Inactive FW revision and HW revision
132-137	6	Supported link length	Supported lengths of various fiber media
138-141	4	Wavelength Information	(for single wavelength modules)
142	1	Supported Pages	
143-144	2	Durations Advertisements	
145-154	10	Module Characteristics	
155-156	2	Supported Controls	
157-158	2	Supported Flags	
159-160	2	Supported Monitors	
161-162	2		Reserved
163-166	4	Supported CDB Functionality	

167-169	3		Reserved
170-175	7		Reserved
176-190	15		Reserved
191-222	32		Custom
223-250	28		Reserved
251-254	4		Reserved
255	1	PageChecksum	Page Checksum over bytes 130-254

8.5.4.1 Inactive Firmware and Hardware Revisions

Table 8-38 describes the fields for reporting the module's inactive firmware revision (if any) and the module's 12 hardware revision.

Note: The active firmware revision is reported in the Module Active Firmware Version fields (see Section 8.5.2.9) and the overall module revision number is reported in the Vendor Revision Number field (see Section 8.5.3.2).

The inactive firmware is that firmware stored that is not currently executing, when the module supports a second firmware image.

Note: This inactive firmware image may be an alternate or backup firmware image, or a new firmware image downloaded but not yet activated.

The ModuleInactiveFirmwareMajorRevision and ModuleInactiveFirmwareMinorRevision fields contain numbers with the same encoding as the ModuleActiveFirmwareMajorRevision and ModuleActiveFirmwareMinorRevision fields (see Section 8.5.2.9): a module without inactive firmware clears these fields.

Bytes 01h:128-29 are not included in the Page 01h Page Checksum as these bytes may change dynamically for modules that support switching firmware version between multiple images during firmware updates.

The numeric ModuleHardwareMajorRevision and ModuleHardwareMinorRevision fields contain version numbers. These two fields are included in the Page 01h Page Checksum.

Table 8-38 Module Inactive Firmware and Hardware Revisions (Page 01h)

Byte	Size	Name	Description
128	All	ModuleInactiveFirmwareMajorRevision	U8 Numeric representation of module inactive firmware major revision
129	All	ModuleInactiveFirmwareMinorRevision	U8 Numeric representation of module inactive firmware minor revision
130	All	ModuleHardwareMajorRevision	U8 Numeric representation of module hardware major revision
131	All	ModuleHardwareMinorRevision	U8 Numeric representation of module hardware minor revision

8.5.4.2 Supported Link Length

The Bytes described in Table 8-39 advertise the maximum supported fiber media length for each type of fiber media at the maximum module-supported bit rate for modules with a separable optical media interface. Unsupported media

types shall be populated with zeroes.

Table 8-39 Supported Fiber Link Length (Page 01h)

Byte	Size	Name	Description
132	7-6	LengthMultiplierSMF	Link length multiplier for SMF fiber 00 = 0.1 (0.1 to 6.3 km) 01 = 1 (1 to 63 km) 10 = 10 (10 to 630 km) 11 = reserved
	5-0	BaseLengthSMF	Base link length for SMF fiber in km. Must be multiplied by multiplier defined in bits 7-6 to calculate actual link length.
133	All	LengthOM5	Link length supported for OM5 fiber, units of 2 m (2 to 510 m)
134	All	LengthOM4	Link length supported for OM4 fiber, units of 2 m (2 to 510 m)
135	All	LengthOM3	Link length supported for EBW 50/125 μm fiber (OM3), units of 2m (2 to 510 m)
136	All	LengthOM2	Link length supported for 50/125 μm fiber (OM2), units of 1m (1 to 255 m)
137	All	LengthPMF	Link length supported for PMF fiber, units of 1cm (1 to 2.55 m)

The link length supported for SMF fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using single mode fiber. The value is in units of kilometers.

The link length supported for OM5 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 4700 MHz*km (850 nm) and 2470 MHz*km (953 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM4 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 4700 MHz*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM3 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 2000 MHz*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM2 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 500 MHz*km (850 nm and 1310 nm) 50 micron multi-mode fiber. The value is in units of one meter.

The link length supported for PMF fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 500 MHz*km (850 nm and 1310 nm) polarization maintaining fiber;. The value is in units of 1 micron meter.

8.5.4.3 Wavelength Information

The NominalWavelength and WavelengthTolerance fields are defined for single wavelength modules.

Note: Nominal wavelength and wavelength tolerance are attributes of optical media lanes, whereas NominalWavelength and WavelengthTolerance are module level fields.

Note: All optical modules, whether single or multiple wavelengths, advertise their supported media specifications indirectly via the MediaInterfaceID of the relevant Application. In many of these Applications, fixed nominal wavelengths and maximum tolerances are known from the associated standard.

A single wavelength module with implicitly defined fixed wavelength and tolerance reports these specified values or more specific actual values (e.g. tighter tolerance).

A single wavelength module with (directly or indirectly) programmable wavelength reports actual nominal wavelength and actual wavelength tolerance.

A multi-wavelength module may optionally provide wavelength information, either for one of the wavelengths or for the entire wavelength range (as nominal center wavelength and overall tolerance). Since the interpretation is not uniquely defined, a host may ignore this field for multi-wavelength modules and use the advertised Application to determine module capabilities.

Table 8-40 Wavelength Information (Page 01h)

Byte	Size	Name	Description
138-139	All	NominalWavelength	U16 nominal transmitter output wavelength for a single wavelength module at room temperature in units of 0.05nm
140-141	All	WavelengthTolerance	U16 wavelength tolerance tol as the worst case +/-tol range around the NominalWavelength under all normal operating conditions in units of 0.005nm

8.5.4.4 Supported Pages Advertising

Table 8-41 Supported Pages Advertising (Page 01h)

Byte	Size	Name	Description
142	7		Reserved
	6	VDMPagesSupported	VDM Pages 20h-2Fh (partially) supported (advertisement details in Page 2Fh)
	5	DiagnosticPagesSupported	Banked Page 13h-14h supported
	4	Page06hSupported	PELS Module Advertising Page 06h is supported
	3	Page05hSupported	Form Factor specific Page 05h is supported
	2	Page05hSupported	User Page 03h supported
	1-0	BanksSupported	Banks supported for Pages 10h-2Fh 00b: Bank 0 supported (8 lanes) 01b: Banks 0 and 1 supported (16 lanes) 10b: Banks 0-3 supported (32 lanes) 11b: reserved

8.5.4.5 Durations Advertising

The ModSelWaitTime numerical value is represented in a special floating-point format by the two fields ModSelWaitTimeMantissa and ModSelWaitTimeExponent and defines both the required setup time (for the ModSel signal after the host asserts ModSel and before the start of an MCI bus transaction) and the required delay (after completion of an MCI transaction before the host can deassert the ModSel signal).

For example, if the module wait time is 1.6 ms, the mantissa field (bits 4-0) value will be 11001b (25) and the exponent field (bits 7-5) value will be 110b (6) for a result of 25·26 = 1600 us. Note that the representation of a ModSelWaitTime value may be ambiguous, e.g. 8 = 1·23 = 2·22 = 4·21 = 8·20.

Table 8-42 Durations Advertising (Page 01h)

Byte	Size	Name	Description
143	7-5	ModSelWaitTimeExponent e	ModSelWaitTime value represented as m·2e in µs 00h: no data available
	4-0	ModSelWaitTimeMantissa m	
144	All		Reserved

Table 8-43 State Duration Encoding (Page 01h)

Encoding	Maximum State Duration T_{state}
0000b	T_{state} < 1 ms
0001b	1 ms <= T_{state} < 5 ms
0010b	5 ms <= T_{state} < 10 ms
0011b	10 ms <= T_{state} < 50 ms
0100b	50 ms <= T_{state} < 100 ms
0101b	100 ms <= T_{state} < 500 ms
0110b	500 ms <= T_{state} < 1 s
0111b	1 s <= T_{state} < 5 s
1000b	5 s <= T_{state} < 10 s
1001b	10 s <= T_{state} < 1 min
1010b	1 min <= T_{state} < 5 min
1011b	5 min <= T_{state} < 10 min
1100b	10 min <= T_{state} < 50 min
1101b	T_{state} >= 50 min
1110b	Reserved
1111b	Reserved

8.5.4.6 Module Characteristics Advertising

The fields in Table 8-44 describe the characteristics of certain module properties. Some features are optional. Advertisement of the implementation of optional features is described in Sections 8.5.7 through 8.5.9.

A LD synchronous group is defined as a LD input lane or group of LD input lanes sourced from the same clock domain. Two different LD synchronous groups may be sourced from different clock domains. There may be a limit on the maximum permissible clock tolerance between two different LD synchronous groups, as defined by the industry standard associated with a given Application. Refer to applicable industry standards.

A LD synchronous group can contain one or more Data Paths, if the LD lanes on all Data Paths are sourced from the same clock domain and the module takes measures to ensure that active Data Paths continue to operate undisturbed even as other Data Paths (and their associated LD input lanes) are enabled/disabled by the host.

Table 8-44 Module Characteristics Advertising (Page 01h)

Byte	Size	Name	Description
145	7	CoolingImplemented	0b: Uncooled transmitter device 1b: Cooled transmitter
	6-5		Reserved
	4		Reserved
	3		Reserved
	2	Aux3MonObservable	0b: Aux 3 monitor monitors Laser Temperature 1b: Aux 3 monitor monitors Vcc2
	1	Aux3MonObservable	0b: Aux 2 monitor monitors Laser Temperature 1b: Aux 2 monitor monitors TEC current
	0	Aux3MonObservable	0b: Aux 1 monitor is custom 1b: Aux 1 monitor monitors TEC current
146	All	ModuleTempMax	S8 Maximum allowed module case temperature in 1 deg C increments. ModuleTempMax = ModuleTempMin = 0 indicates ‘not specified’.
147	All	ModuleTempMin	S8 Minimum allowed module case temperature in 1 deg C increments. ModuleTempMax = ModuleTempMin = 0 indicates ‘not specified’.
148-149	All		Reserved
150	All	OperatingVoltageMin	U8 Minimum supported module operating voltage, in 20 mV increments (0-5.1 V), or zero for ‘not specified’.
151	7-2		Reserved
	1	LDDisableIsFast	0b: Module responds to LD Output Disable with regular timing 1b: Module responds to LD Output Disable in “fast mode” timing limits Refer to form factor hardware specification for regular and “fast mode” timing limit requirements
	0	LDDisableIsModuleWide	0b: LD output disable is controlled per lane 1b: All LD output lanes disabled when any OutputDisableLD set
152-154	All		Reserved

8.5.4.7 Supported Controls Advertisement

Table 8-45 describes supported module and lane controls and related module functions.

Table 8-45 Supported Controls Advertisement (Page 01h)

Byte	Size	Name	Description
155	7	WavelengthIsControllable	0b: No wavelength control 1b: Active wavelength control supported Note: Active Control does not imply tunability
	6	TransmitterIsTunable	0b: Transmitter not tunable 1b: Transmitter is tunable (Pages 04h & 12h supported)
	5-2		Reserved
	1	OutputDisableLDSupported	0b/1b: Host cannot/can disable LD outputs using the OutputDisableLD register
	0		Reserved
156	7	BankBroadcastSupported	0b/1b: The BankBroadcastEnable control is not supported/supported
	6-0		Reserved
157	7-2		Reserved
	1	LOSFlagLDSupported	0b: LD Loss of Signal Flags not supported 1b: supported
	0	FailureFlagLDSupported	0b: LD Fault Flags not supported 1b: supported
158	All		Reserved

8.5.4.8 Supported Monitors Advertisement

Table 8-46 describes supported module and lane monitors.

Table 8-46 Supported Monitors Advertisement (Page 01h)

Byte	Size	Name	Description
159	7-6		Reserved
	5	CustomMonSupported	0b: Custom monitor not supported 1b: Custom monitor supported
	4	Aux3MonSupported	0b: Aux 3 monitor not supported 1b: Aux 3 monitor supported
	3	Aux2MonSupported	0b: Aux 2 monitor not supported 1b: Aux 2 monitor supported
	2	Aux1MonSupported	0b: Aux 1 monitor not supported 1b: Aux 1 monitor supported
	1	VccMonSupported	0b: Internal 3.3 V monitor not supported 1b: Internal 3.3 V monitor supported
	0	TempMonSupported	0b: Temperature monitor not supported 1b: Temperature monitor supported
160	7-5		Reserved
	4-3	LDBiasCurrentScalingFactor	Multiplier for 20 uA Bias current increment used in LD

			Bias current monitor and threshold registers (see Table 8-51) 00b: multiply x1 01b: multiply x2 10b: multiply x4 11b: reserved
	2		Reserved
	1	LDOpticalPowerMonSupported	0b: LD Output Optical Power monitor not supported 1b: LD Output Optical Power monitor supported
	0	LDBiasMonSupported	0b: LD Bias monitor not supported 1b: LD Bias monitor supported

8.5.4.9 CDB Messaging Support Advertisement

Table 8-47 describes how the module advertises fundamental support of the Command Data Block (CDB) command and reply messaging functionality, as well as of some high-level CDB features and characteristics.

Table 8-47 CDB Advertisement (Page 01h)

Byte	Size	Name	Description
163	7-6	CdbInstancesSupported	00b: CDB functionality not supported 01b: One CDB instance supported 10b: Two CDB instances supported 11b: Reserved One CDB Instance Bank 0 of Pages 9Fh and the subset of Pages A0h-AFh advertised in CdbMaxPagesEPL (01h:163.3-0), CdbCmdCompleteFlag1 Flag (00h:8.6) and the associated Mask (00h:31.6) are supported. Two CDB Instances Banks 0 and 1 of Pages 9Fh and of the subset of Pages A0h-Afh advertised in CdbMaxPagesEPL (01h:163.3-0),CdbCmdCompleteFlag<i> (00h:8.7-6), <i> = 1,2, and the associated Masks (00h:31.7-6) are supported.
	5	CdbBackgroundModeSupported	0b: Background CDB operation not supported. 1b: Background CDB operation supported Note: In Background Mode, register access is possible while a CDB command is still being processed.
	4	CdbAutoPagingSupported	When the Management Memory current address pointer advances past the end of an Extended Payload (EPL) CDB Page (A0h-Afh), the page number in the PageSelect Byte will automatically increment and the Memory Map current address pointer automatically wraps to 128. When

<table>
<tr><td></td><td></td><td></td><td>the last page number Afh is incremented, the page number wraps back to A0h.
0b: Auto Paging not supported
1b: Auto Paging and Auto Page wrap supported</td></tr>
<tr><td></td><td>3-0</td><td>CdbMaxPagesEPL</td><td>This field encodes the EPL Page range supported or, equivalently, the maximum length of extended payload:
Value Supported Total Number of
EPL Pages Pages EPL Bytes
0: (none) 0 0
<table><tr><td>Value</td><td>Supported EPL Pages</td><td>Total Pages</td><td>Number of EPL Bytes</td></tr><tr><td>0</td><td>(none)</td><td>0</td><td>0</td></tr><tr><td>1</td><td>A0h</td><td>1</td><td>128</td></tr><tr><td>2</td><td>A0h-A1h</td><td>2</td><td>256</td></tr><tr><td>3</td><td>A0h-A2h</td><td>3</td><td>384</td></tr><tr><td>4</td><td>A0h-A3h</td><td>4</td><td>512</td></tr><tr><td>5</td><td>A0h-A7h</td><td>8</td><td>1024</td></tr><tr><td>6</td><td>A0h-Abh</td><td>12</td><td>1536</td></tr><tr><td>7</td><td>A0h-Afh</td><td>16</td><td>2048</td></tr></table>
Note: A host can access all supported EPL Pages and the EPL Page range is sufficient for all supported CDB commands. The required number of EPL pages may be CDB command specific.</td></tr>
<tr><td>164</td><td>All</td><td>CdbReadWriteLengthExtension</td><td>Note: For READ and WRITE efficiency in CDB messaging, a module can support multi-byte ACCESS in the CDB Page range (9Fh-Afh) with more than 8 bytes.
CdbReadWriteLengthExtension = i specifies i*8 allowable additional number of bytes in a WRITE or READ access to an EPL CDB Page (A0Fh-Afh), i.e. i is a length extension in units of byte octets (8 bytes).
For page 9Fh (without auto paging support), the allowable length extension is min(i,15)*8 = 120 Bytes.
This leads to the maximum length of a READ or a WRITE
<table><tr><td>Value</td><td>Maximum number of bytes (EPL)</td></tr><tr><td>0</td><td>8 bytes (no extension of general length limit)</td></tr><tr><td>i</td><td>8 * (1+i) bytes (0 ≤ i ≤ 255)</td></tr><tr><td>255</td><td>8 * 256 = 2048 bytes max</td></tr><tr><td>Value</td><td>Maximum number of bytes (LPL)</td></tr><tr><td>0</td><td>8 bytes (no extension of general length limit)</td></tr></table></td></tr>
</table>

			i 8 * (1+i) bytes (0 ≤ i ≤ 15) i i: 8 * 16 = 128 bytes (16≤ i ≤ 256) Note: If the MCI transaction from the host is longer than the length allowed as per this advertisement, the module may ignore bytes written beyond the allowed length and not return more that so many bytes in a read.
165	7	CdbCommandTriggerMethod	Determines how the host triggers CDB command processing in the module and when this occurs: 1b: when the MCI transaction of a WRITE access including the CMDID register 9Fh:129 is properly terminated by the host (STOP). 0b: when a single byte WRITE to 9Fh:129 or a two-byte WRITE to the CMDID register Byte 9Fh:128-129 is properly terminated by the host (STOP). Note: Preferred method 1b enables the host to WRITE a complete CMD message (header and body) in one go, whereas in Method 0b the host composes the CMD message body first and then triggers CMD processing in a second step.
	6-5		Reserved
	4-0	CdbExtMaxBusyTime	When CdbMaxBusySpecMethod=1b: CdbExtMaxBusyTime = X encodes the maximum CDB busy time T_{CDBB} as max(1,X)*160 ms in a range of 160 ms to 4960 ms. When CdbMaxBusySpecMethod=0b: don't care
166	7	CdbMaxBusySpecMethod	0b: Indicates that the maximum CDB busy time T_{CDBB} is specified via CdbMaxBusyTime (01h:166.6-0) 1b: Indicates that the maximum CDB busy time T_{CDBB} is specified via CdbExtMaxBusyTime (01h:165.4-0).
	6-0	CdbMaxBusyTime	When CdbMaxBusySpecMethod=0b: CdbMaxBusyTime=X encodes the maximum CDB busy time T_{CDBB} as (80–max(80,X))ms in a range of 0 ms to 80 ms. When CdbMaxBusySpecMethod=1b: don't care

CDB instances, are supported by the module.

A value of CdbInstancesSupported = 0 indicates that CDB is not supported at all.

A CDB instance is identified by non-zero CDB instance number

The Bank Index of the Pages belonging to a CDB instance is the CDB instance number decremented by one.

All CDB instances behave identically and support the same set of CDB commands.

Note: Module support for multiple CDB instances can be useful when long-duration CDB commands operating in

the background are supported, such as firmware update.

Background Operation

The CdbBackgroundModeSupported Bit 01h:163.5 defines if the host can ACCESS the addressable management memory while a CDB command is being processed by the module.

• If CdbBackgroundModeSupported is cleared, the module will hold-off ACCESS while a CDB command is being executed until the command is completed.

• If CdbBackgroundModeSupported is set, the module will possibly hold-off ACCESS only until the CDB command is parsed and captured or queued.

When CDB Background Operation is supported, the host can read the CdbStatus field to determine the status of in-progress CDB commands (see Table 8-21).

While a CDB Command is being executed in the background, the module ensures that the relevant internal background operations (such as flash EEPROM writes) do not affect other host interactions with the module that may concurrently occur in the foreground.

Auto Paging

The advertisements of Auto-Paging support (in CdbAutoPagingSupported Bit 01h:163.4), the number of supported EPL pages (in CdbMaxPagesEPL Field 01h:163.3-0), and the maximum write transaction length (in the CdbReadWriteLengthExtension Byte 01h:164) are interrelated, as described in Table 8-48, below.

Table 8-48 Overview of CDB advertising combinations

Auto Paging Supported? (01h:163.4)	# EPL Pages Supported? (01h:163.3-0)	Max # Bytes in Seq. Byte Write (01h:164)	Description
0	> 0	any	Auto paging is not supported. Normal wrap of current address within page. The host should not write past the end of an EPL Page.
1	0	any	Invalid (useless).
	> 0		Auto Paging is supported, a write past address 255 automatically increments the Page number and wraps the current address pointer to byte 128. If the Page number increment is past the last supported EPL Page, the Page number wraps back to A0h. Note: The host may use the Auto Paging feature to write data in large chunks, without the overhead of explicitly programming Page changes.

8.5.4.10 Page Checksum (Page 01h, Byte 255, RO RQD)

The Page Checksum is a one-byte code that can be used to verify that the read-only static data on Page 01h is valid. The checksum code shall be the low order 8 bits of the arithmetic sum of all byte values from byte 130 to byte 254,

inclusive.

8.5.5 Page 02h (Module and Lane Thresholds)

Page 02h is an optional Page that informs about module-defined thresholds for module-level and lane-specific threshold crossing monitors. All fields on Page 02h are **Read-Only and static**.

The module advertises support of Page 02h in the MemoryModel Bit 00h:2.7.

Note: Page 02h is mandatory for paged memory modules.

Table 8-49 Page 02h Overview

Byte	Size	Subject Area	Description
128-175	48	Module-level monitor thresholds	
176-199	24	Lane-specific monitor thresholds	
200-229	30		Reserved
230-254	25		Custom
255	1	Page Checksum	Covers bytes 128-254

8.5.5.1 Module-Level Monitor Thresholds

The following thresholds are provided by the module to inform the host of the monitored observable levels where alarms and warnings will be triggered.

Table 8-50 Module-Level Monitor Thresholds (Page 02h)

Byte	Bit	Name	Description
128-129	All	TempMonHighAlarmThreshold	S16 Thresholds for internal temperature monitor: 1/256 degree Celsius increments
130-131	All	TempMonLowAlarmThreshold	
132-133	All	TempMonHighWarningThreshold	
134-135	All	TempMonLowWarningThreshold	
136-137	All	VccMonHighAlarmThreshold	U16 Thresholds for internal 3.3 volt input supply voltage monitor: 100 µV increments
138-139	All	VccMonLowAlarmThreshold	
140-141	All	VccMonHighWarningThreshold	
142-143	All	VccMonLowWarningThreshold	
144-145	All	Aux1MonHighAlarmThreshold	S16 Thresholds for TEC Current monitor or custom Aux 1 monitor TEC Current: 100/32767% increments of maximum TEC current +32767 (100%) – Max Heating -32767 (-100%) – Max Cooling
146-147	All	Aux1MonLowAlarmThreshold	
148-149	All	Aux1MonHighWarningThreshold	
150-151	All	Aux1MonLowWarningThreshold	
152-153	All	Aux2MonHighAlarmThreshold	S16 Thresholds for TEC Current or Laser

154-155	All	Aux2MonLowAlarmThreshold	Temperature monitor TEC Current: 100/32767% increments of maximum TEC current +32767 (100%) – Max Heating -32767 (-100%) – Max Cooling Laser Temperature: 1/256 degree Celsius increments
156-157	All	Aux2MonHighWarningThreshold	
158-159	All	Aux2MonLowWarningThreshold	
160-161	All	Aux3MonHighAlarmThreshold	S16 Thresholds for Laser Temperature or additional supply voltage monitor Laser Temperature: 1/256 degree Celsius increments NOTE: Laser Temp can be below 0 if uncooled or in LD Output Disable. Additional supply voltage monitor: 100 µV increments
162-163	All	Aux3MonLowAlarmThreshold	
164-165	All	Aux3MonHighWarningThreshold	
166-167	All	Aux3MonLowWarningThreshold	
168-169	All	CustomMonHighAlarmThreshold	S16 or U16 Custom monitor
170-171	All	CustomMonLowAlarmThreshold	
172-173	All	CustomMonHighWarningThreshold	
174-175	All	CustomMonLowWarningThreshold	

8.5.5.2 Lane-Related Monitor Thresholds

The following thresholds are provided by the module to inform the host of the monitor levels where alarms and warnings will be triggered. These monitor thresholds apply to all lanes of the module.

Table 8-51 Lane-Related Monitor Thresholds (Page 02h)

Byte	Bit	Name	Description
176-177	All	OpticalPowerLDHighAlarmThreshold	U16 Thresholds for LD optical power monitor: in 10uW increments Total measurement range of 0 to 655.35 mW (~-20 dBm to +28.162 dBm for non-zero values)
178-179	All	OpticalPowerLDLowAlarmThreshold	
180-181	All	OpticalPowerLDHighWarningThreshold	
182-183	All	OpticalPowerLDLowWarningThreshold	
184-185	All	LaserBiasCurrentHighAlarmThreshold	U16 Thresholds for LD laser bias monitor: 20 uA increments, times the multiplier encoded in 01h:160.4-3 (see Table 8-46)
186-187	All	LaserBiasCurrentLowAlarmThreshold	
188-189	All	LaserBiasCurrentHighWarningThreshold	
190-191	All	LaserBiasCurrentLowWarningThreshold	
192-199	All		Reserved

8.5.5.3 Page Checksum (Page 02h, Byte 255, RO RQD)

The Page Checksum code is a one-byte code that can be used to verify that the device property information in the module is valid. The Page Checksum code shall be the low order 8 bits of the arithmetic sum of all byte values from byte 128 to byte 254, inclusive.

8.5.6 Page 03h (User EEPROM)

Page 03h is an optional Page that allows the module to provide access to a host writeable EEPROM.

The module advertises support of Page 03h in Bit 01h:142.2 (see Table 8-41).

The host may read or write to this memory for any purpose.

Note: Actual usage of the EEPROM is not standardized by CMIS.

The maximum number of bytes in one WRITE access is 8 bytes.

The module rejects register ACCESS until a WRITE to EEPROM is completed internally.

Note: In SFF-8636, a CLEI code may be present in the first 10 Bytes of Page 03h. In CMIS, this convention is aborted, because the CLEI code is allocated in Bytes 00h:190-199.

8.5.7 Page 05h (Form Factor Specific Management Signals Management)

Page 05h is an optional Page that is restricted for the management of form factor specific management signals, i.e. to form factor specific extensions of the MSL.

The actual specifications are defined in one or more separate OIF documents.

The module advertises support of Page 05h in Bit 01h:142.3 (see Table 8-41).

8.5.8 Page 06h (LD Lane Control)

Page 06h is a Page that contains lane control bytes.

The module advertises support of Page 06h in the MemoryModel Bit 00h:2.7.

Note: Page 0:06h is mandatory for paged memory modules.

Page 06h is subdivided into several areas as illustrated Table 8-18 in Section 8.5.2.5, and detail definitions are given in the following Table 8-52.

The LD lane controls act on individual lanes in the module

Note: The LD lane control settings are not staged and not part of Control Sets.

Note: Readers should carefully distinguish the muting functions (disabling or squelching an output) and the control of these functions that may be exercised by the module itself or by the external host. The effect of both host and module controlling these muting functions depends on advertised module capabilities and on host-controlled configuration

LD Output Disable Function

When an optical LD output is disabled, its output signal has negligible optical average output power as defined by the relevant media interface standard (e.g. average power <-20dBm). The output is then quiescent.

Note: It is irrelevant if the implementation disables transmitter facilities (e.g. laser off) or just shuts down the output. That is why the function is named LD Output Disable instead of LD Disable as in earlier revisions.

When an electrical LD output is disabled, it is quiescent.

Joint Control of LD Output Disable Function

The LD output disable function in the module is normally controlled by the host only, but the DPSM may override and keep an LD output disabled when it is already nominally un-disabled by the host.

LD Output Controls

The host can disable and un-disable LD output lane N using OutputDisableLD<N>.

Table 8-52 Page 06h detail definitions

Upper page 06H				
Byte	Bit	Name	Description	Type
128	7, 0-6 reserved	Programmable Output Power Supported	Indicates Lane support for programmable output power.	RO OPT.
129	0-7	Min. Prog. Output Power MSB	Minimum Programmable Output Power, 16-bit signed value in increment of 0.01 dBm.	RO OPT.
130		Min. Prog. Output Power LSB		
131		Max. Prog. Output Power MSB	Maximum Programmable Output Power, 16-bit signed value in increments of 0.01 dBm	RO OPT.
132		Max. Prog. Output Power LSB		
133	0-7	Lane power monitor high warning threshold MSB	Threshold for Lane optical power: unsigned integer in 10 uW increments, yielding a total measurement range of 0 to 655.35 mW (~-20 to +28.162 dBm)	RO OPT.
134	0-7	Lane power monitor high warning threshold LSB		
135	0-7	Lane power monitor Low warning threshold MSB		
136	0-7	Lane power monitor Low warning threshold LSB		
137	0-7	Lane power monitor high alarm threshold MSB		
138	0-7	Lane power monitor high alarm threshold LSB		
139	0-7	Lane power monitor Low alarm threshold MSB		
140	0-7	Lane power monitor Low alarm threshold LSB		
141	0-7	Lane bais monitor high warning threshold MSB	Lane bias threshold, unsigned integer in 20 uA increments, times the multiplier from Table 8-46. See	RO OPT.

			Section 8.5.9 for monitor details including accuracy	
142	0-7	Lane bais monitor high warning threshold LSB		
143	0-7	Lane bais monitor Low warning threshold MSB		
144	0-7	Lane bais monitor Low warning threshold LSB		
145	0-7	Lane bais monitor high alarm threshold MSB		
146	0-7	Lane bais monitor high alarm threshold LSB		
147	0-7	Lane bais monitor Low alarm threshold MSB		
148	0-7	Lane bais monitor Low alarm threshold LSB		
149-150	0-7	Reserve		
151	bit 7-2	Reserve		
	bit 1	LaserDisableIsFast	0b: Module responds to Laser Output Disable with regular timing 1b: Module responds to Laser Output Disable in regular timing details including accuracyctor hardware specification for regular and in regular timing details including RO OPT.	RO OPT.
	bit 0	LaserDisableIsModuleWide	0b: Laser output disable is controlled per lane 1b: All Laser output lanes disabled when any OutputDisableLaser set	RO OPT.
152-153	0-7	Reserve		
154	bit 7-2	Reserve		
	bit 1	PELS control mode	0b: Module responds to Laser Output Disable with regular timing 1b: Module responds to Laser Output Disable in regular timing limits Refer to form factor hardware specification for regular and “fast mode” timing limit requirements	RO OPT.
	bit 0	Reserve		
155	bit 7-2	Reserve		
	bit 1	OutputDisableLaserSupported	0b/1b: Host cannot/can disable Laser	RO

			outputs using the OutputDisableLaser register	OPT.
	bit 0	Reserve		
156	0-7	Reserve		
157	bit 7-2	Reserve		
	bit 1	LOSFlagLaserSupported	0b: Laser Loss of Signal Flags not supported 1b: supported	RO OPT.
	bit 0	FailureFlagLaserSupported	0b: Laser Fault Flags not supported 1b: supported	RO OPT.
158-159	0-7	Reserve		
160	bit 7-6	Reserve		
	bit 5-3	LaserBiasCurrentScalingFactor	Multiplier for 20uA Bias current increment used in Laser Bias current monitor and threshold registers (see Table 8-45 and Table 8-47) 000b: multiply x1 001b: multiply x2 010b: multiply x4 011b: multiply x8 100b-111b: reserved	RO OPT.
	bit 2	Reserve		
	bit 1	LaserOpticalPowerMonSupported	0b: Laser Output Optical Power monitor not supported 1b: Laser Output Optical Power monitor supported	RO OPT.
	bit 0	LaserBiasMonSupported	0b: Laser Bias monitor not supported 1b: Laser Bias monitor supported	RO OPT.
161	0-7	ModuleFactoryPowerRoomTemperature	Module Factory set power at room(25°C) and high(40~50°C) temperature: unsigned integer in 100 mW increments, yielding a total measurement range of 0 to 25.5W	RO OPT.
162	0-7	ModuleFactoryPowerHighTemperature		RO OPT.
163-171	0-7	LasersFactorySetBiasRoomTemperature	Lasers Factory set bias at room (25°C) and high (40~50°C) temperature: unsigned integer in 10 mA increments, times the multiplier, yielding a total measurement range of 0 to 2.55A	RO OPT.
172-180	0-7	LasersFactorySetBiasHighTemperature		RO OPT.

181-220		Reserve		
221-254	0-7	Custom		
255	1	Page Checksum	Covers bytes 128-254	RO OPT.

8.5.9 Banked Page 1Ah (LD Lane Status and Control)

Page 1Ah is a Page that contains lane status information.

Page 1Ah may optionally be Banked. Each Bank of Page 1Ah refers to a group of 8 lanes.

The module advertises support of Page 1Ah in the MemoryModel Bit 00h:2.7.

Page 1Ah is subdivided into several areas as illustrated in Table 8-11 in Section 8.5.1.

This section of the Memory Map contains lane-specific Flags. These Flags provide a mechanism for reporting operating failures, alarms and warnings for monitored observables, or event occurrences. Each lane-specific Flag has an associated Mask.

The general behavior of Flags, Masks, and Interrupt generation is described in Table 8-12 in Section 8.5.1. With the lane-specific Flags are defined in Table 8-53.

Real time lane monitoring may be performed for each LD output optical power, and LD bias current.

The monitored observables defined here all have associated alarm and/or warning thresholds with associated threshold crossing alarm and/or warning Flags and Flags.

Alarm threshold values and warning threshold values have the same numerical value representation as the associated monitor values for which they specify threshold values.

Measured LD laser bias current is represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 to 65535) with LSB equal to 20 uA times the multiplier from Byte 01h:160. For a multiplier of 1, this yields a total measurement range of 0 to 1310 mA.

Accuracy is Vendor Specific but must be better than +/-10% of the manufacturer's nominal value over specified operating temperature and voltage.

Measured LD optical power is the average power represented in mW. The parameter is encoded as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with LSB equal to 10uW, yielding a total measurement range of 0 to 655.35 mW (~-20 to +28.162 dBm).

Accuracy is Vendor Specific but shall be better than +/-1 dB over specified temperature and voltage for the vendor specified wavelength.

Table 8-53 Page 1Ah detail definitions

Upper page 1Ah				
Byte	Bit	Name	Description	Type
128	7-0	Lane1 Wavelength	Output wavelength at	RO

129	7-0		room temperature, The laser wavelength value is equal to the 16-bit integer value of the wavelength in nm divided by 20 (units of 0.05nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected Applications	
130	7-0	Lane2 Wavelength		
131	7-0			
132	7-0	Lane3 Wavelength		
133	7-0			
134	7-0	Lane4 Wavelength		
135	7-0			
136	7-0	Lane5 Wavelength		
137	7-0			
138	7-0	Lane6 Wavelength		
139	7-0			
140	7-0	Lane7 Wavelength		
141	7-0			
142	7-0	Lane8 Wavelength		
143	7-0			
144	7-0	Lane1 Optical Power MSB	Lane optical power: unsigned integer in 10 uW increments, yielding a total measurement range of 0 to 655.35 mW (~-20 to +28.162 dBm) See Section 8.5.9 for monitor details including accuracy	RO
145	7-0	Lane1 Optical Power LSB		
146	7-0	Lane2 Optical Power MSB		
147	7-0	Lane2 Optical Power LSB		
148	7-0	Lane3 Optical Power MSB		
149	7-0	Lane3 Optical Power LSB		
150	7-0	Lane4 Optical Power MSB		
151	7-0	Lane4 Optical Power LSB		
152	7-0	Lane5 Optical Power MSB		
153	7-0	Lane5 Optical Power LSB		
154	7-0	Lane6 Optical Power MSB		
155	7-0	Lane6 Optical Power LSB		
156	7-0	Lane7 Optical Power MSB		
157	7-0	Lane7 Optical Power LSB		
158	7-0	Lane8 Optical Power MSB		
159	7-0	Lane8 Optical Power LSB		
160	7-0	Lane1 Bias MSB	Lane bias unsigned integer in 20 uA increments, times the multiplier from Table 8-46. See Section 8.5.9 for monitor details including accuracy	RO
161	7-0	Lane1 Bias LSB		
162	7-0	Lane2 Bias MSB		
163	7-0	Lane2 Bias LSB		
164	7-0	Lane3 Bias MSB		
165	7-0	Lane3 Bias LSB		
166	7-0	Lane4 Bias MSB		
167	7-0	Lane4 Bias LSB		
168	7-0	Lane5 Bias MSB		
169	7-0	Lane5 Bias LSB		

170	7-0	Lane6 Bias MSB		
171	7-0	Lane6 Bias LSB		
172	7-0	Lane7 Bias MSB		
173	7-0	Lane7 Bias LSB		
174	7-0	Lane8 Bias MSB		
175	7-0	Lane8 Bias LSB		
176	7-0	Lane Fault flag	Clear on Read	RO,Clear on Read
177	7-0	Lane power High alarm flag		
178	7-0	Lane power low alarm flag		
179	7-0	Lane power High warning flag		
180	7-0	Lane power Low warning flag		
181	7-0	Lane bias High alarm flag		
182	7-0	Lane bias low alarm flag		
183	7-0	Lane bias High warning flag		
184	7-0	Lane bias Low warning flag		
185-192		Reserved		
193-200	7-0	Lane1-8 LaserFactorySetBiasRoomTemperature	Lane# Laser Factory set bias at room (25℃) and high (40~50℃) temperature: unsigned integer in 10mA increments, times the multiplier. yielding a total measurement range of 0 to 2.55A	RW
201-208	7-0	Lane1-8 LasersFactorySetBiasHighTemperature		RW
209	7-0	Lane1 Target output power MSB	Target output power Lane optical power:unsigned integer in 10 uW increments, yielding a total measurement range of 0 to 655.35 mW (~-20 to +28.162 dBm) See Section 8.5.9 for monitor details including accuracy	RW
210	7-0	Lane1 Target output power LSB		
211	7-0	Lane2 Target output power MSB		
212	7-0	Lane2 Target output power LSB		
213	7-0	Lane3 Target output power MSB		
214	7-0	Lane3 Target output power LSB		
215	7-0	Lane4 Target output power MSB		
216	7-0	Lane4 Target output power LSB		
217	7-0	Lane5 Target output power MSB		
218	7-0	Lane5 Target output power LSB		
219	7-0	Lane6 Target output power MSB		
220	7-0	Lane6 Target output power LSB		
221	7-0	Lane7 Target output power MSB		
222	7-0	Lane7 Target output power LSB		
223	7-0	Lane8 Target output power MSB		

224	7-0	Lane8 Target output power LSB		
225	7-0	Output Check	The check byte for each output lane to confirm no dirty on the fiber output. 0b = default value, mean the the check process is fault for each lane. 1b = default value, mean the the check process is passed.	RW
226	7-0	Lane 1-8 disable	0b= Output enabled for lane 1-8 1b= Output disabled for lane 1-8	RW
227	7-0	Lane1-Lane8 Fault flag mask	Masking bit for Lane Fault flag	RW
228	7-0	Lane1-Lane8 Power High Alarm flag mask	Masking bit for Power High Alarm flag mask	RW
229	7-0	Lane1-Lane8 Power Low Alarm flag mask	Masking bit for Power Low Alarm flag mask	RW
230	7-0	Lane1-Lane8 Power High Warning flag mask	Masking bit for Power High Warning flag mask	RW
231	7-0	Lane1-Lane8 Power Low Warning flag mask	Masking bit for Power Low Warning flag mask	RW
232	7-0	Lane1-Lane8 Bias High Alarm flag mask	Masking bit for Bias High Alarm flag mask	RW
233	7-0	Lane1-Lane8 Bias Low Alarm flag mask	Masking bit for Bias Low Alarm flag mask	RW
234	7-0	Lane1-Lane8 Bias High Warning flag mask	Masking bit for Bias High Warning flag mask	RW
235	7-0	Lane1-Lane8 Bias Low Warning flag mask	Masking bit for Bias Low Warning flag mask	RW
236-255		Custom		

9 Measurement Method

9.1 Test Points

The OIO PELS has optical and electrical interfaces to be tested, as listed as TPo and TPe in Figure 9.1. The TPo is at the output end of a PMF fiber patch cord, which is at the length around 1~2 meters. The TPe is the electrical input of the PELS E/O hybrid connector. The used PMF patch cord with connector should have a known PER and insertion loss to further calibrate the measured results of the test equipment.

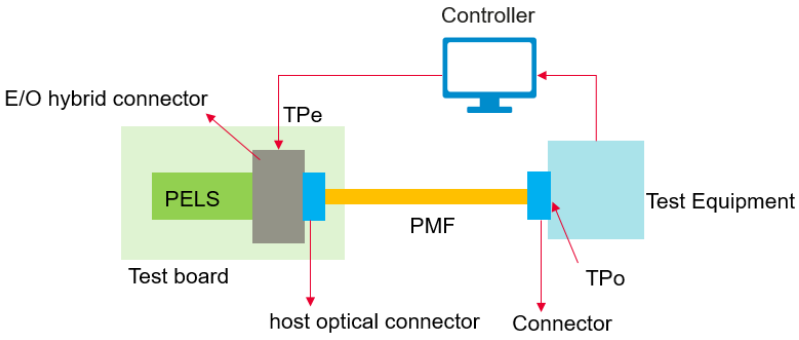


Figure 9.1 OIO PELS test points

9.2 Test Setup for Optical Specifications

For the optical parameters such as optical power, wavelength, laser linewidth, RIN, PER, et.al, one can refer to traditional test setups from corresponding test equipment suppliers.

10 References

10.1 OIF CPO FD 1.0

10.2 OIF CPO 3.2T Module IA 1.0

10.3 OIF ELSFP IA 1.0

10.4 OIF CMIS 5.3

10.5 QSFP, QSFP-DD and QSFP112 MSA

10.6 SFF-8024

Appendix

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